Service Manual

Tektronix

CTS 710 SONET Test Set &
CTS 750 SDH Test Set

070-8853-02

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

CE

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of three (3) years from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEKTRONIX WITH RESPECT TO THIS PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

Injury Precautions

Use Proper Power Cord To avoid fire hazard, use only the power cord specified for this product.

Avoid Electric Overload To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Ground the Product This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in Explosive Atmosphere To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Wear Eye Protection To avoid eye injury, wear eye protection if there is a possibility of exposure to high-intensity rays.

Product Damage Precautions

Use Proper Power Source Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:

DANGER
High Voltage

Protective Ground
(Earth) Terminal

ATTENTION
Refer to
Manual

Double
Insulated

Certifications and Compliances

CSA Certified Power Cords

CSA Certification includes the products and power cords appropriate for use in the North America power network. All other power cords supplied are approved for the country of use.

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Caution When Servicing the CRT

To avoid electric shock or injury, use extreme caution when handling the CRT. Only qualified personnel familiar with CRT servicing procedures and precautions should remove or install the CRT.

CRTs retain hazardous voltages for long periods of time after power is turned off. Before attempting any servicing, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode. Rough handling may cause the CRT to implode. Do not nick or scratch the glass or subject it to undue pressure when removing or installing it. When handling the CRT, wear safety goggles and heavy gloves for protection.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

X-Radiation

To avoid x-radiation exposure, do not modify or otherwise alter the high-voltage circuitry or the CRT enclosure. X-ray emissions generated within this product have been sufficiently shielded.

Preface

This manual explains how to verify, service, troubleshoot, and repair the CTS 700-Series Test Set (CTS) to the module level.

Information in this manual applies equally to the CTS 710 SONET Test Set and the CTS 750 SDH Test Set unless otherwise specified.

The manual contains the following information:

- *Specifications* lists the instrument specifications. A complete set of specifications is provided for both the SONET and SDH versions of the CTS 700-Series Test Set.
- *Operating Information* provides instruction on installation and gives you a brief summary of operating the CTS. If you need further assistance operating the CTS, refer to the user manual supplied with the instrument.
- *Theory of Operation* provides general descriptions of system unit modules, sufficient to guide the technician to a faulty module.
- *Performance Verification* describes how to verify the functional performance of the CTS.
- *Adjustment Procedures* describes how to perform adjustments on the CTS.
- *Maintenance* includes procedures for the following:
  - Inspection and cleaning
  - General troubleshooting
  - Module removal and replacement
- *Options* lists the options to the CTS.
- *Electrical Parts List* provides some general information about replaceable parts for the CTS.
- *Diagrams* contains an interconnect diagram and a block diagram of CTS modules.
- *Mechanical Parts List* describes the replaceable parts for the CTS.
- *Glossary* lists terms used by the CTS or this manual.

Conventions

The following conventions apply throughout this manual:

- Each test procedure begins with a table, similar to the one below, that provides information you need to know before starting the test.

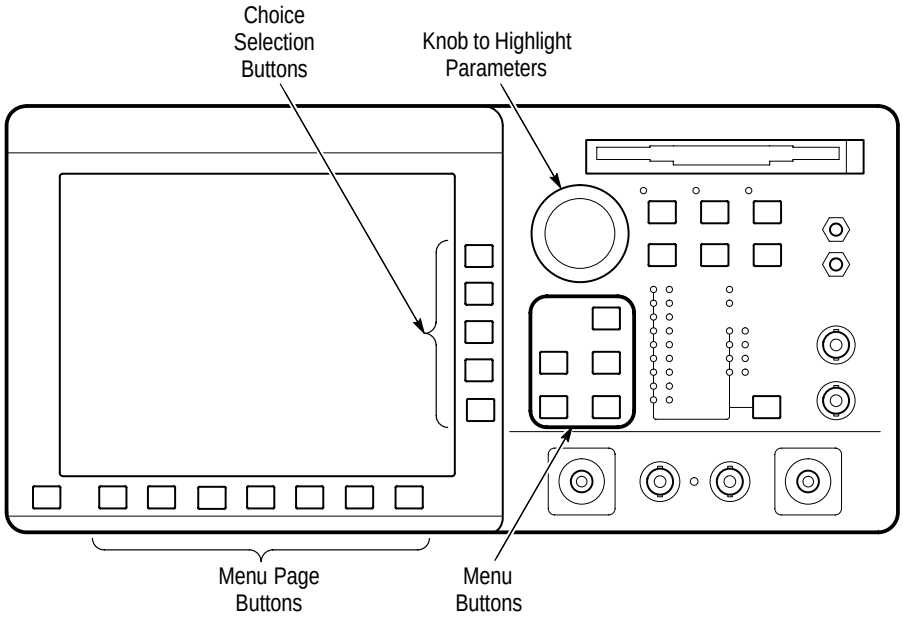
Equipment Required	Communications Signal Analyzer (item 4) 75 Ω coaxial cable (item 19) Delay line (item 24), three required
Prerequisites	Prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

  The item numbers after each piece of equipment refer to line numbers in Table 4–2, *Required Test Equipment*, which begins on page 4–4.

- This manual presents setup instructions for the CTS in tables. Perform the steps reading from left to right in the table (see example below).

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
Begin here with Step 1	Step 2	Step 3	Step 4
		Step 5	Step 6
		Step 7	Step 8, CTS setup is complete

  Menu buttons are located on the instrument front panel (see illustration on the next page). Select menu pages with the buttons below the display. Use the knob to highlight a parameter; then use the buttons at the right side to select a choice. Many setups require several iterations of highlighting parameters and selecting choices. Some setups may require more than one menu button or menu page selection as well.



Related Manuals

These other manuals are available for the CTS 700-Series Test Set:

- The *CTS 710 SONET Test Set User Manual* and *CTS 750 SDH Test Set User Manual* (part numbers 070-8852-XX and 070-8921-XX, respectively) provide a tutorial and detailed operating instructions.
- The *CTS 710 SONET Test Set & CTS 750 SDH Test Set Reference* (part number 070-8975-XX) provides a quick overview of the menu structure and front-panel buttons.
- The *CTS 710 SONET Test Set Programmer Manual* and *CTS 750 SDH Test Set Programmer Manual* (part numbers 070-8924-XX and 070-8925–XX, respectively) describe how to control the CTS using an instrument controller.
- The *CTS 710 SONET Test Set & CTS 750 SDH Test Set Reference* (part number 070-8854-XX) provides a quick overview of the instrument programming commands.

Introduction

This manual contains all the information needed for periodic maintenance of the CTS 700-Series Test Set. (Examples of such information are procedures for checking performance and for adjustment.) Further, it contains all information for repair to the board or module level. This means that the procedures, diagrams, and other troubleshooting aids help isolate failures to a specific module, rather than to components of that module. Once a failure is isolated, replace the module with a replacement or exchange module obtained from Tektronix.

All modules are listed in the *Mechanical Parts List* section. To isolate a failure to a board or module, use the fault isolation procedures found in the *Maintenance* section. To remove and replace any failed board or module, follow the instructions in *Removal and Replacement Procedures*, also found in *Maintenance*.

Service Offerings

Tektronix provides service to cover repair under warranty. Other services are available that can provide a cost-effective answer to your service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians, trained on Tektronix products, are best equipped to service your CTS 700-Series Test Set. Tektronix technicians are apprised of the latest information on improvements to the product as well as the latest product options.

Warranty Repair Service

Tektronix technicians provide warranty service at most Tektronix service locations worldwide. (The warranty appears after the title page and copyright page in this manual.) Your Tektronix product catalog lists all service locations worldwide.

Repair Service

The following services can be purchased to tailor repair of your CTS 700-Series Test Set to fit your requirements.

Depot Service. Tektronix offers single per-incident repair and annual maintenance agreements that provide repair of the CTS.

Of these services, the annual maintenance agreement offers a particularly cost-effective approach to service for many owners of the CTS 700-Series Test Set. Such agreements can be purchased to span several years.

Self Service

Tektronix supports repair to the module level by offering a *Module Exchange* program.

Module Exchange. This service reduces down time for repair by allowing you to exchange most modules for remanufactured ones. Tektronix ships you an updated and tested exchange module from the Beaverton, Oregon service center. Each module comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the repair or adjustment services previously described.

Before You Begin

This manual is for servicing the CTS 700-Series Test Set. To prevent injury to yourself or damage to the instrument, do the following tasks before you attempt service:

- Read the Safety Summaries found at the beginning of this manual
- Read *Service Offerings* in this section

When using this manual to service your CTS 700-Series Test Set, be sure to heed all warnings, cautions, and notes.

Specifications

This section begins with a brief description of the CTS 700-Series Test Sets. Following the description, the section contains a complete listing of the instrument specifications.

Product Description

The CTS 700-Series Test Sets are rugged, portable test sets designed for installing and maintaining telecommunications networks. The CTS 710 SONET Test Set and CTS 750 SDH Test Set combine bit error rate test capabilities with overhead testing, payload mapping, and demapping in one unit. The CTS test sets feature the following capabilities (options are required for some features):

- STS-1, STS-3, OC-1, OC-3, and OC-12 transmit and receive (CTS 710)
- STM-1 and STM-4 transmit and receive (CTS 750)
- DS1/DS3 Add/Drop/Test (with CTS 710 Option 22)
- 2, 34, and 140 Mb/s Add/Drop/Test (with CTS 750 Option 36)
- Bit Error Rate testing
- BIP error monitoring and analysis
- Payload mapping and demapping
- Alarm generation and analysis
- APS testing
- DCC and user channel access
- Programmable via IEEE 488.2 and RS-232
- Jitter generation and analysis (with CTS 750 Option 14)
- Wander generation and measurement (with CTS 750 Option 14)

The CTS test sets meet the needs of the craftsperson and the network engineer. The instruments meet the requirements of those working in network installation and maintenance by providing the following capabilities:

- Network integrity testing
- In-service performance monitoring
- Stimulus and response testing

- Stress testing
- Overhead testing

Guide to the Specifications

The following sections contain the complete specifications for the CTS 700-Series Test Sets. The first section contains the CTS 710 specifications. The next section, beginning on page 1–17, covers the specifications for the CTS 750.

All specifications are warranted unless they are designated *typical*. Warranted characteristics that are directly checked by a procedure contained in the *Performance Verification* section of this manual are marked with a ✓ symbol.

If the characteristic is noted as *typical*, the characteristic is not warranted. Typical characteristics describe typical or average performance and provide useful reference information.

Performance Conditions

The electrical characteristics found in these tables apply when the CTS has been adjusted at an ambient temperature between +20° C and +30° C, has been warmed up for at least 20 minutes, and is being operated at an ambient temperature between 0° C and +50° C (unless otherwise noted).

CTS 710 Specification Tables

The CTS 710 SONET Test Set specifications, as referenced to the ANSI and Bellcore SONET standards, are arranged by functional groups in Tables 1–1 through 1–5.

Table 1–1: Standard CTS 710 Specifications

Characteristic	Description
Generator Output	
Electrical Output	
Data Rates	STS-1: 51.84 Mb/s STS-3: 155.52 Mb/s
Data Formats	STS-1: AMI, B3ZS STS-3/STS-3c: CMI
⩘ Signal Level at Transmit Output	STS-1 Hi: $\pm$1.0 V_{pk} $\pm$10% into 75 Ω STSX-1: with 450 feet of cable loss STS-3 Hi: $\pm$0.5 V_{pk} $\pm$10% into 75 Ω STSX-3: with 225 feet of cable loss
⩘ Pulse Shape at Transmit Output	Meets ANSI T1-102, Bellcore GR-NWT-000253 Eye Pattern Masks
Return Loss	>15 dB, with instrument power on
Output Protection	Open and short circuit protected
Connector	Unbalanced, 75 Ω BNC
Optical Output	
Data Rates	OC-1: 51.84 Mb/s OC-3: 155.52 Mb/s OC-12: 622.08 Mb/s
Data Format	Scrambled NRZ
Optical Module Options	Opt. 03: 1310 nm, IR, OC-1/3 Opt. 04: 1310 nm, IR, OC-1/3/12 Opt. 05: 1550 nm, LR, OC-1/3/12 Opt. 06: 1310/1550 nm, OC-1/3/12
Signal Level & Wavelength	Opt. 03, 04, 06: –10 dBm, typical 1310 nm Opt. 05, 06: 0 dBm, typical, 1550 nm
⩘ Pulse Shape	Meets Bellcore GR-253-CORE Eye Pattern Masks
Wavelength	1308 nm, typical (Opt. 03, 04, 06) 1550 nm, typical (Opt. 05, 06)
Spectral Width	≤ 4 nm, 1310 nm (Opt. 03, 04, 06) ≤ 1 nm, 1550 nm (Opt. 05, 06)
Extinction Ratio	≥ 10 dB
Laser Classification	Class 1 laser, complies with 21 CFR 1040.10 and 1040.11, complies with IEC 825, Section 9.4
Connectors	FC-PC Standard (optical connector kit with ST, SC, and DIN 47256 included)

Table 1–1: Standard CTS 710 Specifications (Cont.)

Characteristic	Description
Signal Structure	
✓ Standards Compliance	Meets the requirements of ANSI T1.105A, Section 8 and Bellcore GR-NWT-000253
Payload Channel (SPE)	One active STS-1 in STS-3 Selection (The other 2 channels are unequipped) One active STS-1 in STS-12 (The other 11 channels are unequipped) One active STS-3c in STS-12 (The other 3 channels are unequipped)
Unequipped Payload	C2 byte is set to 00
Internal Pattern Generator	
Patterns Bulk Fill in a selected SPE channel (STS-1 or STS-3c)	PRBS: 2^9–1, 2^{15}–1, 2^{20}–1, 2^{23}–1; All 1s, All 0s, 8-bit programmable word
Errors Single or Continuous	Section BIP (B1) Line BIP (B2) Path BIP (B3), Path FEBE Payload pattern bit
Error Rate Range	1×10^{-3} to 1×10^{-10} with 0.1 resolution (depends on error type)
Alarms	Line AIS, Line FERF Path AIS, Path FERF
✓ Failures	LOS, LOF, LOP
Transmitter Clock	
Internal Clock	
✓ Accuracy	±4.6 ppm, for instrument calibrated within 24 months
Line Output Jitter	< 0.01 UI_{RMS} in the frequency band between 12 kHz and 5 MHz (complies with Bellcore TR-NWT-000253, Sections 5.6.1 and 5.6.5.2; and Bellcore TR-NWT-000499, Section 7.3.3)
External Clock Reference	
✓ Rate	1.544 MHz ±40 ppm
Input	Balanced, 100 Ω ±5%, Bantam connector
Recovered Clock	
Loop timing	Clock is recovered from received signal
✓ Frequency lock range	Nominal line rate ± 125 ppm
Transmit Line Frequency Offset	
✓ Frequency offset rate	±100 ppm of nominal line rate
Receive Input	
Electrical Input	
Data Rates	STS-1: 51.84 Mb/s ±100 ppm STS-3: 155.52 Mb/s ±100 ppm
Data Formats	STS-1E: AMI, B3ZS coded STS-3/STS-3c: CMI

Table 1–1: Standard CTS 710 Specifications (Cont.)

Characteristic	Description
✓ Signal Sensitivity	STS-1 Hi: 0.5 Vpk min to 1.2 Vpk max STSX-1: 0.25 Vpk min to 0.6 Vpk max STS-1 Lo: 0.125 Vpk min to 0.35 Vpk max STS-1 Monitor: 20 dB of flat loss below Xcon STS-3: 0.35 Vpk min to 0.6 Vpk max STSX-3: 0.35 Vpk min to 0.6 Vpk max STS-3 Lo: 0.07 Vpk min to 0.3 Vpk max STS-3 Monitor: 26 dB of flat loss below Hi
Signal Level Display	Readout for electrical signal level in mV
Signal Equalization	STS-1: Cross-connect equalization for 450 feet of AT&T 728A cable Low-level equalization for 900 feet of AT&T 728A cable STS-3: Automatic equalization for 0 to 450 feet of cable loss to ITU-T Rec. G.708 and ANSI TI-102
Return Loss	>15 dB, with instrument power on
Input Protection	Up to ± 5V, short term
Connector	Unbalanced, 75 Ω BNC
Optical Input	
Data Rates	OC-1: 51.84 Mb/s (±100 ppm) OC-3: 155.52 Mb/s (±100 ppm) OC-12: 622.08 Mb/s (±100 ppm)
Data Format	Scrambled NRZ
Maximum Input Power	–7 dBm (Opt. 05 and 06 include a 10 dB attenuator)
Operating Wavelength	1310 nm and 1550 nm (1100 nm to 1570 nm operating range)
✓ Signal Sensitivity	–28 dBm for BER $\leq 10^{-10}$
Optical Power Meter Accuracy	2 dBm, typical (for input power in a range of –30 dBm to –6 dBm)
Connectors	FC-PC standard (optical connector kit with ST, SC, and DIN 27256 included)
Through Mode	Monitors a selected channel and passes the signal through unchanged.
Transmit and Receive Functional Specifications	
Transport Overhead	
Access	Set overhead bytes to any value from binary 00000000 to 11111111: A1, A2, C1, E1, F1, D1–D3, K1, K2, D4–D12, S1, Z2, M2, E2 View all Transport Overhead bytes
Add/Drop	Insert data from the Overhead Add/Drop connector into the Section DCC, Line DCC or F1 user byte. Drops data from the Section DCC, Line DCC, or F1 user byte out to the Overhead Add/Drop connector.
K1 and K2 (APS)	Set the APS Bytes, K1 and K2, to any code defined in ANSI T1.105A. Selectable by text description for all Span and Ring messages.

Table 1–1: Standard CTS 710 Specifications (Cont.)

Characteristic	Description
Path Overhead	
Access	Set Path Overhead bytes to any value from binary 00000000 to 11111111: C2, F2, Z3, Z4, and Z5 View all Path Overhead bytes
Add/Drop	Insert data from the Overhead Add/Drop connector into the F2 user byte. Drop data from the F2 user byte out to the Overhead Add/Drop connector.
Path Trace Byte J1	Send user-defined 64-byte sequence, or set to 00000000 View Path Trace J1
Pointer Movement	
Single	Single pointer justification (increment or decrement)
Burst	Bursts of two to eight pointer justifications spaced four frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions.
✓ Continuous	Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 2 ms to 10 s, with a resolution of 1 ms.
Set to Value	Set to a new location with or without the NDF being set. Range is 0 to 1023 (783 – 1023 are illegal locations).
Pointer Test Sequences	
Single pointer adjustment	Time between pointer adjustments: 30 s.
Alternating pointer adjustment	Alternating, single Alternate, double
Pointer adjustment burst	Time between 3 pointers is 0.5 ms, 0.5 ms Time between pointer burst: 30 s
Phase transient pointer adjustment burst	Time between 7 pointers is 0.25 s, 0.25 s, 0.5 s, 0.5 s, 0.5 s, 0.5 s. Time between pointer bursts: 30 s.
Periodic pointer adjustment – 87–3 pattern	– 87–3 pattern – 87–3 pattern with cancelled pointer movement number 87 – 87–3 pattern with added pointer after the 43rd pointer
Periodic pointer adjustment – continuous pattern	– continuous pattern – continuous pattern with cancellation of one pointer – continuous pattern with added pointer
Pointer Direction	Positive or Negative
Initialization Period	On or Off Thirty second burst of 1 pointer per second in the same direction as the selected test.
Cool Down Period	On or Off This will last at least 60 seconds.

Table 1–1: Standard CTS 710 Specifications (Cont.)

Characteristic	Description
Measurements	
Error Count, Error Rate, and Errored Seconds for	B1, B2, B3, Payload, Line-FEBE, Path-FEBE
Alarm and Failure Seconds	LOS, OOF, LOF, SPE LOP, Line AIS & FERF, Path AIS & FERF, Loss of Power, Loss of Pattern Sync
STS SPE Pointer Measurements	Seconds: LOP, Illegal pointers, NDF Count: Illegal pointers, Positive justifications, Negative justifications
T1M1.3 Analysis	
Section B1 Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors
Line B2 & FEBE Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS FEBE-Count, FEBE-ES, FEBE-UAS, FEBE-EFS
Path B3 & FEBE Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS FEBE-Count, FEBE-ES, FEBE-UAS, FEBE-EFS
Pattern Bit Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS
LEDs	
Status Indicators	LOS, LOF, LOP, Line AIS, Line FERF, Path AIS, Path FERF, Errors, Pointer Adjust, Signal Present, Pattern Lock
Histograms	
Error Count, Bit Error Rate and Errored Seconds	B1, B2, B3, Line-FEBE, Path-FEBE, Pattern Bit
Alarms & Failures On/Off	LOS, OOF, LOF, SPE-LOP, Line-AIS, Line-FERF, Path-AIS, Path-FERF, Pattern Loss, Loss of Power
Pointers	STS Pointer Value, Pointer Justification
Measurement Utilities	
Measurement Control	Manual Start/Stop Timed: 1 s to 99 days with 1 s resolution Continuous
Histogram Display Resolution	1 min, 5 min, 15 min, 1 hour (displays 72 hours with 1 min resolution) 15 min, 60 min, 4 hrs, 12 hrs (displays 45 days with 15 min resolution)
Result Logging	All measurements are recorded with start, stop time and date. The current and previous results are stored in memory both totalized and graphical. Both graphical and totalized results can be stored on a disk.

Table 1–1: Standard CTS 710 Specifications (Cont.)

Characteristic	Description
Utilities	
TroubleScan	Scans all measurement results for key violations.
AutoScan	AutoScan to incoming signal (rate, mapping, framing, and pattern). Identifies incoming signal and presents graphical display of SPE and VT structure. Identifies VT signal status by showing VT number, equipped vs unequipped, alarms and pattern.
Stored Setups	5 front panel setups in memory 200 front panel setups per disk
Pass/Fail Tests	Predefined Pass/Fail Tests can be created, stored and executed Pass/Fail tests are stored on disk 200 Pass/Fail test setups per disk
Add/Drop Interface for Data Communication Channels and User Channels	A DB-37 female connector provides the interface to an external protocol analyzer. Clock and data signals are differential TTL, conform to RS-422 specifications, and are also compatible with single-ended TTL signals. Add/Drop: D1–D3, D4–D12, F1, F2 Connector: 37 Pin DIN (DTE and DCE)
Triggering	Pulse at start of each frame, (Tx and Rx) Connector: 37 Pin DIN
Disk Drive	3.5 inch, 1.44 MB, DOS compatible Measurement Result stored in ASCII Stored Setups and Pass/Fail Tests in IEEE 488.2 format
Printer	Optional printer in pouch (thermal): HC 411 Printer support: Epson, HP Thinkjet Serial Printer Port: RS-232 Print to disk: BMP format, Interleaf format, and Encapsulated PostScript
Computer Interface	IEEE-488.2 interface RS-232-C interface (DB9)
Help Mode	Online task-oriented help
Display	7 inch diagonal CRT, magnetic deflection Horizontal raster-scan green phosphor Resolution: 640 by 480 pixels VGA output: 15 pin connector

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities

Characteristic	Description
DS1/DS3 Generator	
Electrical Output	
Data Rates	DS1 (1.544 Mb/s) DS3 (44.736 Mb/s)
Formats	DS1: AMI, B8ZS coded DS3: B3ZS coded
⩘ Signal Level	DS1: 3 V_{pk} ±0.6 V into 100 Ω DS3: 0.6 V_{pk} ±0.24 V into 75 Ω
⩘ Pulse Shape	Meets ANSI T1-102 Pulse Masks
Connectors	DS1: Bantam 100 Ω DS3: BNC 75 Ω
Data Source	DS1: DS1 Generator SONET VT1.5 Drop DS3: DS3 Generator SONET SPE Drop
DS1/DS3 Internal Pattern Generator	
Framing	DS1: SF(D4) ESF Unframed DS3: M13 C-bit Parity Unframed
Patterns	PRBS: 2^{15}–1, 2^{20}–1, 2^{23}–1; All 1's, All 0's, Fixed Pattern 8 bit, Fixed Pattern 16 bit, Fixed Pattern 24 bit, QRSS (DS1 only), 1 in 8 (DS1 only), 3 in 24 (DS1 only)
Errors Single or Continuous	DS1: Frame Bit Error CRC-6 Error (ESF only) Pattern Bit Error DS3: Frame Bit Error P Parity Bit Error (M13 framing only) C Parity Bit Error (C-Bit parity only) Pattern Bit Error
Error Rate Range	1×10^{-2} to 1×10^{-8} with 0.1 resolution (depends on error type)
Alarms and Failures	DS1: Yellow AIS DS3: Yellow AIS (DS3 blue) Idle
VT1.5/DS3 Mapping	
VT1.5 Map Signal Source	Internal DS1 Generator Received DS1 signal
VT1.5 Mapping	Floating Asynch

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities (Cont.)

Characteristic	Description
VT1.5 Active Map Channel Selection	Allows selection of any one of 28 VT channels Remaining 27 VT channels are background
VT1.5 Background Channels	
Background Channel Content	When internal DS1 generator is used: QRSS or Idle pattern (11010101) When external source is used: QRSS
Background Channel Framing	When internal DS1 generator is used: Same as active channel When external source is used: Unframed
VT1.5 Errors (Single or Continuous)	VT BIP-2 VT FEBE
VT1.5 Alarms and Failures	VT AIS VT FERF VT Loss of Pointer VT Loss of Multiframe
DS3 SPE Add Source	Internal DS3 Generator Received DS3 signal
Transmitter Clock	
Internal Clock	
Accuracy	±4.6 ppm, for instrument calibrated within 24 months
External Clock Reference	
Rates	1.544 MHz ±40 ppm
Input	Balanced, 100 Ω ±5%, DS1 Bantam connector
Recovered Clock	
Loop timing	Clock is recovered from received signal
Transmit Line Frequency Offset	
Frequency offset rate	±100 ppm of nominal line rate with 0.1 ppm resolution
External DS1/DS3	Clock Input (for Jitter Generation)
⩘ Rates	1.544 Mb/s, 44.736 Mb/s
Input	Unbalanced, 75 Ω BNC, AC coupled
Signal Level	0.5 volts to 1.5 volts peak to peak

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities (Cont.)

Characteristic	Description
DS1/DS3 Receiver	
Electrical Input	
Data Rates	DS1: (1.544 MHz) ±150 ppm DS3: (44.736 MHz) ±150 ppm
Formats	DS1: AMI, B8ZS DS3: B3ZS
Impedance	DS1: 100 Ω balanced DS1 Bridged: 1 kΩ balanced DS3: 75 Ω to ground, unbalanced
⩘ Signal Level	DSX-1: 3 Vpk ±0.6 V into 100 Ω DS-1 Monitor: 20 dB flat loss below DSX-1 DSX-3: 0.6 Vpk ±0.24 V into 75 Ω DS-3 Monitor: 20 dB flat loss below DSX-3
Connectors	DS1: Bantam 100 Ω DS3: BNC 75 Ω
DS1/DS3 Internal Pattern Receiver	
Pattern Receiver Source	DS1: Rx Signal (ext) VT1.5 Drop DS3: Rx Signal (ext) SONET SPE Drop
Framing	DS1: SF(D4) ESF Unframed DS3: M13 C-bit Parity Unframed
Demultiplexing	
Demux DS3 to DS1	Allows selection of any one of 28 DS1 channels from a DS3
VT1.5/DS3 Demapping	
VT1.5 Demapping	Floating Async
VT1.5 Active Demap Channel Selection	Allows selection of any one of 28 VT channels
Drop VT1.5 to	Internal DS1 Receiver External DS1 signal output
Drop DS3 from	Selected STS-1 Channel
Drop DS3 to	Internal DS3 Receiver External DS3 signal output
VT Path Overhead	
VT1.5 Path Overhead Access	V5 control (—–xxxx–) Set VT Path Overhead bytes to any value from binary 00000000 to 11111111: Z3, Z4, and Z5 View all Path Overhead bytes

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities (Cont.)

Characteristic	Description
VT1.5 Path Trace Byte J2	Send user-defined 16-byte sequence, or set to 00000000 View Path Trace J2
VT Pointer Movement	
VT1.5 Pointer Interaction	VT1.5 or STS, but not both at the same time
Single	Single pointer justification (increment or decrement)
Burst	Bursts of two to eight pointer justifications spaced four multi-frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions.
Continuous	Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 48 ms to 1 s, with a resolution of 1 ms.
Set to Value	Set to a new location with or without the NDF being set. Range is from 0 to 1023 (104 – 1023 are illegal locations).
VT Pointer Test Sequences	
Single pointer adjustment	Time between pointer adjustments: 30 s
Alternating pointer adjustment	Single Double
Pointer adjustment burst	Time between 3 pointers is 2 ms, 2 ms Time between pointer burst: 30 s
Phase transient pointer adjustment burst	Time between 7 pointers is 0.25 s, 0.25 s, 0.5 s, 0.5 s, 0.5 s, 0.5 s Time between pointer bursts: 30 s
Periodic pointer adjustment test sequence – 26–1 pattern	– 26–1 pattern – 26–1 pattern with cancelled pointer movement number 26 – 26–1 pattern with added pointer after the 13th pointer
Periodic pointer adjustment – continuous pattern	– continuous pattern – continuous pattern with cancellation of one pointer – continuous pattern with added pointer
Pointer Direction	Positive or Negative
Initialization Period	On or Off Thirty second burst of 1 pointer per second in the same direction as the selected test.
Cool Down Period	On or Off This will last at least 60 seconds.
Measurements	
DS1 Error Count, Error Rate and Error seconds for	Frame Bit CRC-6 (ESF only) Pattern Bit
DS3 Error Count, Error Rate and Error seconds for	Frame Bit P Parity Bit (M13 framing only) C Parity Bit (C-Bit parity only) Pattern Bit
VT1.5 Error Count, Error Rate and Error seconds for	VT BIP-2 VT FEBE

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities (Cont.)

Characteristic	Description
DS1 Alarm and Failure Seconds for	AIS Yellow Loss of Pattern Sync Loss of Frame Loss of Signal
DS3 Alarm and Failure Seconds for	AIS (DS3 Blue) Yellow (DS3 FERF) Idle Loss of Pattern Sync Loss of Frame Loss of Signal
VT1.5 Alarm and Failure Seconds for	VT AIS VT FERF VT Loss of Pointer VT Loss of Multiframe
VT1.5 Pointer Measurements	Seconds: Count: LOP Illegal pointers Illegal pointers Positive justifications NDF Negative justifications
T1M1.3 Analysis	
VT1.5 BIP-2 & FEBE Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES UAS, EFS, FEBE-Count, FEBE-ES, FEBE-UAS, FEBE-EFS
DS1 Frame Error (SF) & CRC-6 Error (ESF), Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS
DS3 P-Bit Error (M13) & C-Parity Error (C-Bit Parity), Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS
DS1/DS3 Payload (Pattern Bit Errors), Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES,UAS, EFS
LEDs	
Status Indicators	VT AIS DS1/DS3 AIS VT FERF DS1/DS3 YELLOW VT BIP-2 ERROR DS1/DS3 ERROR

Table 1–2: Option 22 DS1/DS3/VT1.5 Capabilities (Cont.)

Characteristic	Description
Histograms for DS1, DS3 and VT1.5	
DS1/DS3/VT1.5 Error Count, Bit Error Rate and Errored Seconds	CRC, Frame, Parity, VT-BIT2, VT-FEBE, Pattern Bit
DS1/DS3/VT1.5 Alarms & Failures On/Off	LOS, LOF, AIS, Yellow (FERF), VT-LOP, VT-AIS, VT-FERF, VT-LOM, Pattern Loss, Loss of Power
VT1.5 Pointers	VT Pointer Value, Pointer Justification
Measurement Utilities	
Measurement Control	Manual Start/Stop Timed: 1 s to 99 days with 1 s resolution Continuous
Histogram Display Resolution	1 min, 5 min, 15 min, 1 hour (displays 72 hours with 1 min resolution) 15 min, 60 min, 4 hrs, 12 hrs (displays 45 days with 15 min resolution)
Result Logging	All measurements are recorded with start, stop time and date. The current and previous results are stored in memory both totalized and graphical. Both graphical and totalized results can be stored on a disk.

Table 1–3: Environmental Specifications

Characteristic	Description	
Temperature	Operating:	0° C to +40° C
	Nonoperating:	–40° C to +75° C
Altitude	Operating:	4,572 m (15,000 ft)
	Nonoperating:	12,192 m (40,000 ft)
Humidity	Operating:	To 95%, relative humidity at or below +40° C for 2 hours or less
		To 90% relative humidity at or below 30° C, continuous
Transportation Handling	Qualifies under National Safe Transit Association 1s Pre-shipment Test; 1A-B-1.	

Table 1–4: Physical Characteristics

Characteristic	Description
Dimensions	Height: 165 mm (6.5 in) 191 mm (7.5 in) with accessory pouch Width: 362 mm (14.25 in) Depth: 490 mm (19.25 in) with front cover 564 mm (22.2 in) with handle extended
Weight	Net: Approximately 8.7 kg (19.3 lb) Shipping: Approximately 14.1 kg (31 lb)
Power Requirements	*Line Voltage* / *Line Frequency* 90 V to 132 V / 50/60 Hz 180 V to 250 V / 50/60 Hz 100 V to 132 V / 400 Hz Maximum current is 6 A_{RMS}.

Table 1–5: Certifications and compliances

Characteristic	Description
EC Declaration of Conformity – EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: EN 55011 Class A Radiated and Conducted Emissions EN 50082-1 Immunity: IEC 801-2 Electrostatic Discharge Immunity IEC 801-3 RF Electromagnetic Field Immunity IEC 801-4 Electrical Fast Transient/Burst Immunity IEC 801-5 Power Line Surge Immunity
FCC Compliance	Emissions comply with FCC Code of Federal Regulations 47, Part 15, Subpart B, Class A Limits
EC Declaration of Conformity – Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities: Low Voltage Directive 73/23/EEC EN 61010-1/A1 Safety requirements for electrical equipment for measurement, control, and laboratory use
Approvals	UL3111-1 – Standard for Electrical Measuring and Test Equipment CAN/CSA C22.2 No. 1010-1 – CSA Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use

Table 1–5: Certifications and compliances (Cont.)

Characteristic	Description	
Conditions for Safety Certification	Operating temperature:	+5 to +40 °C
	Relative Humidity: (maximum operating)	80% up to 31 °C ,decreasing linearly to 50% at 40 °C
	Max. Operating altitude:	2000 m
	Equipment Type:	Test and measuring
	Safety Class:	Class I, grounded product (IEC1010-1)
	Overvoltage Category:	CAT II (IEC1010-1)
	Polution Degree:	Polution Degree 2, rated for indoor use only (IEC1010-1)
Installation Category Descriptions	Terminals on this product may have different installation category designations. The installation categories are:	
	CAT III	Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location
	CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected
	CAT I	Secondary (signal level) or battery operated circuits of electronic equipment

CTS 750 Specification Tables

The CTS 750 SDH Test Set specifications, as referenced to the ITU-T SDH standards, are arranged by functional groups in Tables 1–6 through 1–10.

Table 1–6: Standard CTS 750 Specifications

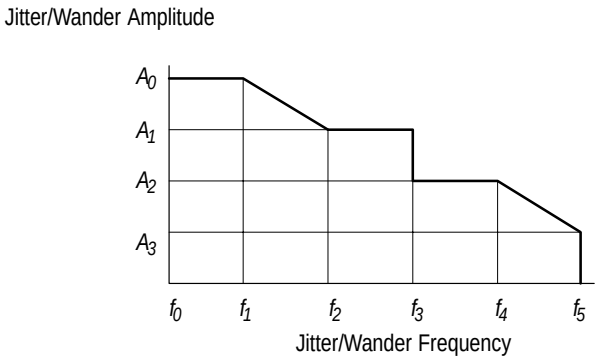
Characteristic	Description
Generator Output	
Electrical Output	
Data Rates	STM-0: 51.84 Mb/s STM-1: 155.52 Mb/s
Data Formats	STM-0E: AMI, B3ZS STM-1E: CMI
⩘ Signal Level at Transmit Output	STM-0E Hi: ±1.0 V_{pk} ±10% into 75 Ω STM-0E: equivalent of –6 dB of cable loss (–12.7 dB √f characteristic cable) STM-1E Hi: ±0.5 V_{pk} ±10% into 75 Ω STM-1E: equivalent of –6 dB of cable loss (–12.7 dB √f characteristic cable)
⩘ Pulse Shape at Transmit Output	Meets ITU-T G.703 Eye Pattern Masks
Return Loss	>15 dB, with instrument power on
Output Protection	Open and short circuit protected
Connector	Unbalanced BNC, 75 Ω to ground
Optical Output	
Data Rates	STM-0: 51.84 Mb/s STM-1: 155.52 Mb/s STM-4: 622.08 Mb/s
Data Format	Scrambled NRZ
Optical Module Options	Opt. 03: 1310 nm, IR, STM-0/1 Opt. 04: 1310 nm, IR, STM-0/1/4 Opt. 05: 1550 nm, LR, STM-0/1/4 Opt. 06: 1310/1550 nm, STM–0/1/4
Signal Level & Wavelength	Opt. 03, 04, 06: –10 dBm, typical 1310 nm Opt. 05, 06: 0 dBm, typical, 1550 nm
⩘ Pulse Shape	Meets ITU-T G.957 Eye Pattern Masks
Wavelength	1308 nm, typical (Opt. 03, 04, 06) 1550 nm, typical (Opt. 05, 06)
Spectral Width	≤ 4 nm, 1310 nm (Opt. 03, 04, 06) ≤ 1 nm, 1550 nm (Opt. 05, 06)
Extinction Ratio	≥ 10 dB
Laser Classification	Class 1 laser, complies with 21 CFR 1040.10 and 1040.11, complies with IEC 825, Section 9.4
Connectors	FC-PC Standard (optical connector kit with ST, SC, and DIN 47256 included)

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Signal Structure	
Standards Compliance	Meets the requirements of ITU-T707, 708, 709
Payload Channel (AU)	One active STM-1 in STM-4 (the other 3 channels are unequipped) One active STM-0 in STM-1 selection (the other 2 channels are unequipped) One active STM-0 in STM-4 (the other 11 channels are unequipped)
Unequipped Payload	C2 byte is set to 00
Internal Pattern Generator	
Patterns Bulk Fill in a selected AU channel (AU3 or AU4)	PRBS: 2^9–1, 2^{15}–1, 2^{20}–1, 2^{23}–1; All 1s, All 0s, 8-bit programmable word
Errors Single or Continuous	RS BIP (B1) MS BIP (B2) Path BIP (B3), Path FEBE Payload pattern bit
Error Rate Range	1×10^{-3} to 1×10^{-10} with 0.1 resolution (depends on error type)
Alarms	MS AIS, MS FERF Path AIS, Path FERF
✓ Failures	LOS, LOF, LOP
Transmitter Clock	
Internal Clock	
✓ Accuracy	±4.6 ppm, for instrument calibrated within 24 months
Line Output Jitter	< 0.01 UI_{RMS} in the frequency band between 12 kHz and 5 MHz (complies with Bellcore TR-NWT-000253, Sections 5.6.1 and 5.6.5.2; and Bellcore TR-NWT-000499, Section 7.3.3)
External Clock Reference	
Rates	2.048 Mb/s ±40 ppm 2.048 MHz ±50 ppm
Input	Unbalanced, 75 Ω ±5%, BNC connector
Recovered Clock	
Loop timing	Clock is recovered from received signal
✓ Frequency lock range	Nominal line rate ± 125 ppm
Transmit Line Frequency Offset	
✓ Frequency offset rate	±100 ppm of nominal line rate

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Jitter Generator (requires Option 14)	
Jittered Line Output	Sinusoidal modulation of transmit clock frequency, applicable to any SDH or PDH data rate. Changes to jitter amplitude or frequency are phase continuous.
Modulation Range	Modulation is selectable up to the following limits, which depend on the rate:



Amplitude Scale in UI_{p-p}	A_0	A_1	A_2	A_3		
All rates	100,000	10	3	1		
Frequency Scale in Hz	f_0	f_1	f_2	f_3	f_4	f_5
2 Mb/s rate	12 µ	30 m	300	9 k	33 k	100 k
34 Mb/s rate	12 µ	30 m	300	10 k	270 k	800 k
140 Mb/s rate	12 µ	30 m	300	20 k	1.2 M	3.5 M
52 Mb/s rate	12 µ	30 m	300	10 k	130 k	400 k
155 Mb/s rate	12 µ	30 m	300	35 k	430 k	1.3 M
622 Mb/s rate	12 µ	30 m	300	125 k	1.7 M	5 M

Amplitude Accuracy, typical	± 5% ± 0.06 UI, at 622 Mb/s rate ± 5% ± 0.03 UI, for all other rates
Frequency Accuracy	± 1%, from 12 µHz to 20 Hz ± 5 ppm, from 20 Hz to f_{max}
Jittered Clock Output	Operates in addition to the jittered line output. Compliant with G.703 2048 kHz synchronization interface specifications.
Output Level, typical	0.8 V_{p-p} output (for all rates) is ECL compatible when terminated with 75 Ω 2 MHz G.703 output is compliant with G.703 2048 kHz synchronization interface specifications
Nominal Data Rates	2 MHz, 34 MHz, 140 MHz, 52 MHz, 155 MHz, or 622 MHz. Same as transmit line or can be set independently (except the 622 Mb/s jittered clock output is not available if the 2 Mb/s transmit rate is selected).
Connector	Rear-panel, unbalanced 75 Ω BNC

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Jitter Clock Input	Input to measure jitter on a clock signal.
Nominal Data Rates	Any supported SDH or PDH rate. Rate is independent of the receive line rate.
Frequency Tolerance	Nominal rate ±100 ppm
Data Format	RZ
Sensitivity, typical	0.4 V_{p-p}
Maximum Input Amplitude	1.5 V_{p-p}
Connector	Rear-panel, unbalanced 75 Ω BNC
Analog Jitter Output	Demodulated jitter from the receiver. The output is filtered by any measurement filters selected.
Connector	Rear-panel 50 Ω BNC
Sensitivity, typical	Normal measurement range: 125 mV/UI Extended measurement range: 3.5 mV/UI
Output Level, typical	± 1V, centered at 0 V ± 100 mV
Receive Input	
Electrical Input	
Data Rates	STM-0: 51.84 Mb/s ±100 ppm STM-1: 155.52 Mb/s ±100 ppm
Data Formats	STM-0E: AMI, B3ZS coded STM-1E: CMI
⩘ Signal Sensitivity/Equalization	STM-0E Hi: 0.5 Vpk min to 1.2 Vpk max STM-0E –6 dB[1]: 0.25 Vpk min to 0.6 Vpk max STM-0E Lo[2]: 0.125 Vpk min to 0.35 Vpk max STM-0E Monitor: 20 dB of flat loss below –6 dB STM-1E Hi: 0.35 Vpk min to 0.6 Vpk max STM-1E –6 dB[3]: 0.35 Vpk min to 0.6 Vpk max STM-1E Lo[4]: 0.07 Vpk min to 0.3 Vpk max STM-1E Monitor: 26 dB of flat loss below Hi
Signal Level Display	Readout for electrical signal level in mV
Return Loss	>15 dB, with instrument power on
Input Protection	Up to ± 5V, short term
Connector	Unbalanced BNC, 75 Ω to ground

1 **–6 dB cable loss @ 25 MHz (–12.7 dB √f characteristic cable)**

2 **–12 dB cable loss @ 25 MHz (–12.7 dB √f characteristic cable)**

3 **–6 dB cable loss @ 78 MHz (–12.7 dB √f characteristic cable)**

4 **–12 dB cable loss @ 78 MHz (–12.7 dB √f characteristic cable)**

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Optical Input	
Data Rates	STM-0: 51.84 Mb/s (±100 ppm) STM-1: 155.52 Mb/s (±100 ppm) STM-4: 622.08 Mb/s (±100 ppm)
Data Format	Scrambled NRZ
Maximum Input Power	–7 dBm (Opt. 05 and 06 include a 10 dB attenuator)
Operating Wavelength	1310 nm and 1550 nm (1100 nm to 1570 nm operating range)
✓ Signal Sensitivity	–28 dBm for BER $\leq 10^{-10}$
Optical Power Meter Accuracy	2 dBm, typical (for input power in a range of –30 dBm to –6 dBm)
Connectors	FC-PC standard (optical connector kit with ST, SC, and DIN 27256 included)
Through Mode	Monitors a selected channel and passes the signal through unchanged
Transmit and Receive Functional Specifications	
Section Overhead	
Access	Set overhead bytes to any value from binary 00000000 to 11111111: A1, A2, C1, E1, F1, D1–D3, K1, K2, D4–D12, S1, Z2, M2, E2 View all Section Overhead bytes
Add/Drop	Insert data from the Overhead Add/Drop connector into the Section DCC, Line DCC or F1 user byte. Drops data from the Section DCC, Line DCC, or F1 user byte out to the Overhead Add/Drop connector.
K1 and K2 (APS)	Set the APS Bytes, K1 and K2, to any code defined in ANSI T1.105A Selectable by text description for all Span and Ring messages
Path Overhead	
Access	Set Path Overhead bytes to any value from binary 00000000 to 11111111: C2, F2, Z3, Z4, and Z5 View all Path Overhead bytes
Add/Drop	Insert data from the Overhead Add/Drop connector into the F2 user byte. Drop data from the F2 user byte out to the Overhead Add/Drop connector.
Path Trace Byte J1	A user-defined string can be transmitted in 64-byte sequence, or set to 00000000
Pointer Movement	
Single	Single pointer justification (increment or decrement)
Burst	Bursts of two to eight pointer justifications spaced four frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions.
✓ Continuous	Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 2 ms to 10 s, with a resolution of 1 ms.

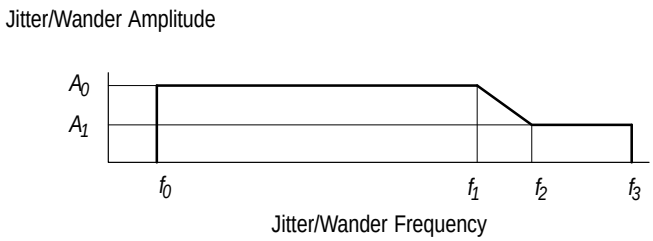
Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Set to Value	Set to a new location with or without the NDF being set. Range is 0 to 1023 (783 – 1023 are illegal locations).
AU Pointer sequences available	G.783(a) Single Alternating G.783(b) Regular + Double G.783(c) Regular + Missing G.783(d) Double Alternating G.783(e) Single G.783(f) Burst G.783(g) Periodic 87–3 G.783(g) Periodic 87–3 With Add G.783(g) Periodic 87–3 With Cancel G.783(h) Periodic G.783(h) Periodic with Add G.783(h) Periodic with Cancel Phase Transient Pointer Adjustment Burst
Initialization Period	On or Off Thirty second burst of 1 pointer per second in the same direction as the selected test.
Cool Down Period	On or Off This will last at least 60 seconds.
Measurements	
Error Count, Error Rate, and Errored Seconds for:	B1, B2, B3, Payload, MS-FEBE, Path-FEBE
Alarm and Failure Seconds for	LOS, OOF, LOF, AU LOP, MIS AIS & FERF, Path AIS & FERF, Loss of Power, Loss of Pattern Sync
AU Pointer Measurements	Seconds: LOP, Illegal pointers, NDF Count: Illegal pointers, Positive justifications, Negative justifications
G.826 Analysis	
RS B1 Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors
MS B2 & FEBE Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors
Path B3 & FEBE Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
G.821 Analysis	
Pattern Bit Seconds and % of total time	Error-Count, ES, SES, UAS, EFS, DM
Section B1 Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors
RS B1 Seconds and ratio	Error Blocks, ES, SES, UAS Background Block Errors
MS B2 & FEBE Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS FEBE-Count, FEBE-ES, FEBE-UAS, FEBE-EFS
Path B3 & FEBE Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS FEBE-Count, FEBE-ES, FEBE-UAS, FEBE-EFS
Pattern Bit Seconds and % of total time	Error-Count, ES, ES-A, ES-B, SES, UAS, EFS
Jitter and Wander Analysis (requires Option 14)	
Jitter Measurements	Peak-to-peak Jitter, Positive Peak Jitter, Negative Peak Jitter, Jitter Hit Seconds, Jitter Out-of-range Seconds Peak-to-peak or RMS jitter measurement of the Clock or Line input. Exceeds the requirements of ITU-T G.783, G.823, G.825, G.958, and O.171.
Video Related Jitter Measurements	Jitter Pointer Event Seconds, Current Frequency Drift Rate, Maximum Frequency Drift Rate
Measurement Filter Response	Measurement filters meet the requirements of ITU-T G.783, G.823, G.825, G.958, and O.171. Lower cutoff (high pass) is first order (–20 dB/decade). Upper cutoff (low pass) is third order (–60 dB/decade) Butterworth. Cutoff frequencies are –3 dB ± 1 dB.
Wideband Filter (–3 dB)	2 Mb/s: 20 Hz to 100 kHz 34 Mb/s: 100 Hz to 800 kHz 140 Mb/s: 200 Hz to 3.5 MHz STM-0E: 100 Hz to 400 kHz STM-1E: 500 Hz to 1.3 MHz STM-1: 500 Hz to 1.3 MHz STM-4: 1 kHz to 5 MHz
Highband Filter (–3 dB)	2 Mb/s (low Q): 18 kHz to 100 kHz 2 Mb/s (high Q): 700 Hz to 100 kHz 34 Mb/s: 10 kHz to 800 kHz 140 Mb/s: 10 kHz to 3.5 MHz STM-0E: 20 kHz to 400 kHz STM-1E: 65 kHz to 1.3 MHz STM-1: 65 kHz to 1.3 MHz STM-4: 250 kHz to 5 MHz

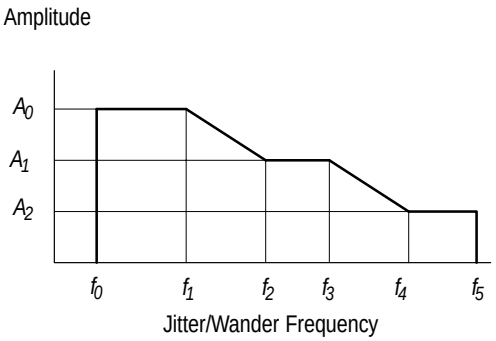
Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Fullband Filter (–3 dB)	2 Mb/s: 10 Hz* to 100 kHz 34 Mb/s: 10 Hz* to 800 kHz 140 Mb/s: 10 Hz* to 3.5 MHz STM-0E: 10 Hz* to 400 kHz STM-1E: 10 Hz* to 1.3 MHz STM-1: 10 Hz* to 1.3 MHz STM-4: 10 Hz* to 5 MHz * Lower –3dB frequency is user selectable to 0.1 Hz, 1 Hz, or 10 Hz.
RMS Filter (–3 dB)	2 Mb/s: 12 kHz to 100 kHz 34 Mb/s: 12 kHz to 800 kHz 140 Mb/s: 12 kHz to 3.5 MHz STM-0E: 12 kHz to 400 kHz STM-1E: 12 kHz to 1.3 MHz STM-1: 12 kHz to 1.3 MHz STM-4: 12 kHz to 5 MHz
Normal Jitter Measurement Resolution and Range	Resolution: 0.005 UI Range: see graph 
Amplitude Scale in UI_{p-p} All rates	A_0: 6 A_1: 0.5 * * A_1 amplitude is 0.3 UI_{p-p} for 2 Mb/s rate with PRBS pattern, and for 622 Mb/s rate with any pattern.

Frequency Scale in Hz	f_0	f_1	f_2	f_3
2 Mb/s rate	0.1	5.3 k	64 k	100 k
34 Mb/s rate	0.1	13.3 k	160 k	800 k
140 Mb/s rate	0.1	26.7 k	320 k	3.5 M
52 Mb/s rate	0.1	26.7 k	320 k	400 k
155 Mb/s rate	0.1	26.7 k	320 k	1.3 M
622 Mb/s rate	0.1	68 k	1.33 M	5 M

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Extended Jitter Measurement Resolution and Range	Resolution: 0.01 UI Range: see graph



Amplitude Scale in UI_{p-p}	A_0	A_1	A_2
All rates	200	16	0.5 *

* A_1 amplitude is 0.3 UI_{p-p} for 2 Mb/s rate with PRBS pattern, and for 622 Mb/s rate with any pattern.

Frequency Scale in Hz	f_0	f_1	f_2	f_3	f_4	f_5
2 Mb/s rate	0.1	30	375	2 k	64 k	100 k
34 Mb/s rate	0.1	30	375	5 k	160 k	800 M
140 Mb/s rate	0.1	30	375	10 k	320 k	3.5 M
52 Mb/s rate	0.1	30	375	10 k	320 k	400 k
155 Mb/s rate	0.1	30	375	10 k	320 k	1.3 M
622 Mb/s rate	0.1	30	375	25 k	1.33 M	5 M

Intrinsic Noise with Jitterless Clock, typical

For peak-to-peak measurement, in UI_{p-p}:

	Highband	*Wideband*	*Fullband (10 Hz)*
2 Mb/s rate	≤0.02	≤0.03	≤0.1
34 Mb/s rate	≤0.02	≤0.03	≤0.1
140 Mb/s rate	≤0.02	≤0.03	≤0.1
52 Mb/s rate	≤0.02	≤0.03	≤0.1
155 Mb/s rate	≤0.02	≤0.03	≤0.1
622 Mb/s rate	≤0.05	≤0.06	≤0.1

For RMS measurement, ≤0.01 UI_{RMS} at all rates

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Intrinsic Noise with Jitterless PRBS Data Signal, typical	For peak-to-peak measurement, in UI_{p-p}:

	Highband	*Wideband*	*Fullband (10 Hz)*	*Fullband (1 Hz)*
2 Mb/s rate	≤0.035	≤0.035	≤0.1	≤0.2
34 Mb/s rate	≤0.035	≤0.035	≤0.1	≤0.2
140 Mb/s rate	≤0.035	≤0.035	≤0.1	≤0.2
52 Mb/s rate	≤0.035	≤0.035	≤0.1	≤0.2
155 Mb/s rate	≤0.035	≤0.035	≤0.1	≤0.2
622 Mb/s rate	≤0.06	≤0.07	≤0.25	≤0.75

For RMS measurement, ≤0.01 UI_{RMS} at all rates

Jitter Measurement Accuracy

Jitter measurement accuracy is a function of the jitter frequency, intrinsic noise in the CTS 750, the filter chosen, and measurement resolution. Measured jitter uncertainty is expressed by the equation below, where f_{LC} is the lower cutoff frequency and f_{UC} is the upper cutoff frequency:

$$Measured\ \ jitter\ \ (f) = Jitter\ \ input\ \ (f) \times \left[\sqrt{\frac{\left(\frac{f}{f_{LC}}\right)^2}{1 + \left(\frac{f}{f_{LC}}\right)^2}} \times \sqrt{\frac{1}{1 + \left(\frac{f}{f_{UC}}\right)^6}} \pm 5\% \right]$$

$$\pm\ Intrinsic\ \ noise\ \pm\ Resolution$$

Additional Corrections to Jitter Measurement Accuracy	2 Mb/s Extended Range, add ±5% 622 Mb/s Extended Range at < 5 °C, substitute ±10% for ±5% in the above equation
Wander Measurements	Estimated Bit Slips, Estimated Frame Slips, Peak-to-peak Wander, TIE (Time Interval Error), Current Frequency, Maximum Frequency, Minimum Frequency
Peak-to-peak Measurement	Range: 1,000,000 ns Noise: ± 5ns Accuracy: 1% ± noise Bandwidth: 0 Hz to 10 Hz
TIE Measurement	Range: 500,000 ns Noise: ± 5ns Accuracy: 1% ± noise Bandwidth: 0 Hz to 10 Hz
Frequency Measurement	Resolution: 1 Hz absolute (0.01 ppm change) Accuracy: ±0.1 ppm (with respect to source clock)
Frequency Drift Measurement	Range: 100 ppm/s Resolution: 0.001 ppm/s Accuracy: 1% ± 0.01 ppm/s Bandwidth: 0 Hz to 0.5 Hz

Table 1–6: Standard CTS 750 Specifications

Characteristic	Description
LEDs	
Status Indicators	LOS, LOF, LOP, MS AIS, MS FERF, Path AIS, Path FERF, Errors, Pointer Adjust, Signal Present, Pattern Lock
Histograms	
Error Count, Bit Error Rate and Errored Seconds	B1, B2, B3, MS-FEBE, Path-FEBE, Pattern Bit
Alarms & Failures On/Off	LOS, OOF, LOF, AU-LOP, MIS-AIS, AU-FERF, Path-AIS, Path-FERF, Pattern Loss, Loss of Power
Pointers	AU Pointer Value, Pointer Justification
Measurement Utilities	
Measurement Control	Manual Start/Stop Timed: 1 s to 99 days with 1 s resolution Continuous
Histogram Display Resolution	1 min, 5 min, 15 min, 1 hour (displays 72 hours with 1 min resolution) 15 min, 60 min, 4 hrs, 12 hrs (displays 45 days with 15 min resolution)
Result Logging	All measurements are recorded with start, stop time and date. The current and previous results are stored in memory both totalized and graphical. Both graphical and totalized results can be stored on a disk.
Utilities	
TroubleScan	Scans all measurement results for key violations.
AutoScan	AutoScan to incoming signal (rate, mapping, framing and pattern). Identifies incoming signal and presents graphical display of AU and TU structure. Identifies TU signal status by showing TU number, equipped vs unequipped, alarms, and pattern.
Stored Setups	5 front panel setups in memory 200 front panel setups per disk
Pass/Fail Tests	Predefined Pass/Fail Tests can be created, stored and executed Pass/Fail tests are stored on disk 200 Pass/Fail test setups per disk
Add/Drop Interface for Data Communication Channels and User Channels	A DB-37 female connector provides the interface to an external protocol analyzer. Clock and data signals are differential TTL, conform to RS-422 specifications, and are also compatible with single-ended TTL signals. Add/Drop: D1–D3, D4–D12, F1, F2 Connector: 37 Pin DIN (DTE and DCE)
Triggering	Pulse at start of each frame, (Tx and Rx) Connector: 37 Pin DIN
Disk Drive	3.5 inch, 1.44 MB, DOS compatible Measurement Result stored in ASCII Stored Setups and Pass/Fail Tests in IEEE 488.2 format

Table 1–6: Standard CTS 750 Specifications (Cont.)

Characteristic	Description
Printer	Optional printer in pouch (thermal): HC 411 Printer support: Epson, HP Thinkjet Serial Printer Port: RS-232 Print to disk: BMP format, Interleaf format, and Encapsulated PostScript
Computer Interface	IEEE-488.2 interface RS-232-C interface (DB9)
Help Mode	Online task-oriented help
Display	7 inch diagonal CRT, magnetic deflection Horizontal raster-scan green phosphor Resolution: 640 by 480 pixels VGA output: 15 pin connector

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities

Characteristic	Description
2 Mb/s, 34 Mb/s, 140 Mb/s Generator	
Electrical Output	
Data Rates	2 Mb/s (2.048 Mb/s) 34 Mb/s (34.368 Mb/s) 140 Mb/s (139.264 Mb/s)
Formats	2 Mb/s: 34 Mb/s: HDB3 coded 140 Mb/s: CMI coded
Signal Level	2 Mb/s: 3 Vpk ±0.6 V into 120 Ω 2 Mb/s: 2.37 Vpk ±0.6 V into 75 Ω 34 Mb/s: 1 Vpk ±0.6 V into 75 Ω 140 Mb/s: 1 Vpk ±0.6 V into 75 Ω
Pulse Shape	Meets ITU-T G.703 Pulse Masks
Connectors	2 Mb/s: 3-pin Siemens 120 Ω 2 Mb/s, 34 Mb/s, 140 Mb/s: BNC 75 Ω
Data Source	2 Mb/s: 2 Mb/s Internal Generator SDH TU12 Drop 34 Mb/s: 34 Mb/s Internal Generator SDH TU3 Drop 140 Mb/s: 140 Mb/s Internal Generator SDH VC4 Drop

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
2 Mb/s, 34 Mb/s, 140 Mb/s Internal Pattern Generator	
Framing	2 Mb/s: PCM30 (CAS) PCM31 PCM30 CRC (CAS) PCM31 CRD Unframed 34 Mb/s and 140 Mb/s: Framed Unframed
Patterns	PRBS: 2^{15}–1, 2^{20}–1, 2^{23}–1; All 1s, All 0s, 1 in 8 (2 Mb/s only); Fixed Pattern: 8 bit, 16 bit, 24 bit
Errors Single or Continuous	Frame Bit Error CRC-4 Error (2 Mb/s only) Pattern Bit Error
Error Rate Range	1×10^{-2} to 1×10^{-8} with 0.1 resolution (depends on error type)
Alarms	RAI AIS
TU12/TU3/VC4 Mapping	
Mapping Signal Source for TU12, TU3, and VC4	Internal Generator: 2 Mb/s 34 Mb/s 140 Mb/s Received Signal: 2 Mb/s 34 Mb/s 140 Mb/s
Mapping mode	Floating Asynch
TU12 Active Map Channel Selection	Allows selection of any one of 63 TU channels Remaining 62 TU channels are background
TU3 Active Map Channel Selection	Allows selection of any one of 3 TU channels Remaining 2 TU channels are background
140 Mb/s Active Map Channel Selection	Into selected STM-1 VC4
TU Background Channels	
TU Background Channel Content	When internal 2 Mb/s or 34 Mb/s generator is used: PRBS: 2^{15}–1 or Idle pattern (11010101) When external source is used: PRBS: 2^{15}–1
Background Channel Framing	When internal 2 Mb/s or 34 Mb/s generator is used: Same as active channel When external source is used: Unframed
TU Errors (Single or Continuous)	TU12 BIP–2 TU12 FEBE TU3 BIP–8 TU3 FEBE
✓ TU Alarms and Failures	TU AIS TU FERF TU Loss of Pointer TU Loss of Multiframe

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
Transmitter Clock	
Internal Clock	
Accuracy	±4.6 ppm, for instrument calibrated within 24 months
External Clock Reference	
✓ Rates	2.048 Mb/s ±40 ppm 2.048 MHz ±50 ppm
Input	Unbalanced, 75 Ω BNC connector
Recovered Clock	
Loop timing	Clock is recovered from received signal
Transmit Line Frequency Offset	
Frequency offset rate	2 Mb/s: ±50 ppm of nominal line rate 34 Mb/s: ±130 ppm of nominal line rate 140 Mb/s: ±100 ppm of nominal line rate with 0.1 ppm resolution
External Reference	±100 ppm of line rate referenced to external source
External PHD Clock Input (for Jitter Generation)	
✓ Rates	2 Mb/s, 34 Mb/s, 140 Mb/s [1] [1] 140 Mb/s rate is not functional if Option 14 is installed
Input	Unbalanced, 75 Ω BNC, AC coupled
Signal Level	0.5 V to 1.5 V peak to peak
Internal Jitter Generator	Refer to *Jitter Generator* on page 1–19

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
2 Mb/s, 140 Mb/s Receiver	
Electrical Input	
Data Rates	2 Mb/s (2.048 Mb/s) ±150 ppm 34 Mb/s (34.368 Mb/s) ±150 ppm 140 Mb/s (139.264 Mb/s) ±150 ppm
Formats	2 Mb/s: HDB3 coded 34 Mb/s: HDB3 coded 140 Mb/s: CMI coded
Impedance	2 Mb/s: 120 Ω balanced 2 Mb/s Bridged: 1 kΩ balanced 2 Mb/s, 34 Mb/s, 140 Mb/s: 75 Ω unbalanced
Signal Level	2 Mb/s: 3 Vpk ±0.6 V into 120 Ω 2.37 Vpk ±0.6 V into 75 Ω Monitor: 26 dB flat loss below Hi 34 Mb/s: 0.6 Vpk ±0.24 V into 75 Ω Monitor: 26 dB flat loss below Hi 140 Mb/s: 0.6 Vpk ±0.24 V into 75 Ω Monitor: 26 dB flat loss below Hi
Connectors	2 Mb/s: 3-pin Siemens 120 Ω 2 Mb/s, 34 Mb/s, 140 Mb/s: BNC 75 Ω
2 Mb/s, 34 Mb/s 140 Mb/s Internal Pattern Receiver	
Pattern Receiver Source	2 Mb/s: 2 Mb/s External Input SDH TU12 Drop 34 Mb/s: 34 Mb/s External Input SDH TU3 Drop 140 Mb/s: 140 Mb/s External Input SDH VC4 Drop
Framing	2 Mb/s: 34 Mb/s and 140 Mb/s: PCM30 (CAS) Framed PCM31 Unframed PCM30 CRC (CAS) PCM31 CRC Unframed
TU12/TU3/VC4 Demapping	
Demapping TU12, TU3 and VC4 Signal Drop to	Internal Receiver: External Signal Output: 2 Mb/s 2 Mb/s 34 Mb/s 34 Mb/s 140 Mb/s 140 Mb/s
Demapping mode	Floating Asynch
TU12 Active Demap Channel Selection	Allows selection of any one of 63 TU channels
TU3 Active Demap Channel Selection	Allows selection of any one of 3 TU channels

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
140 Mb/s Active Demap Channel from	Selected STM-1 VC4
TU Path Overhead	
TU12 Path Overhead Access	V5 control (––xxxx–) Set Path Overhead bytes to any value from binary 00000000 to 11111111: Z3, Z4, and Z5 View all TU Path Overhead bytes
TU3 Path Overhead Access	Set Path Overhead bytes to any value from binary 00000000 to 11111111: C2, F2, Z3, Z4, and Z5 View all TU Path Overhead bytes
TU3 Path Trace Byte J1	Send user-defined 16 or 64-byte sequence, or set to 00000000 View Path Trace J1
TU12 Path Trace Byte J2	Send user-defined 16-byte sequence, or set to 00000000 View Path Trace J2
TU Pointer Measurement	
TU Pointer Interaction	TU12, TU3, or AU, but not at the same time
Single	Single pointer justification (increment or decrement)
Burst	Bursts of two to eight pointer justifications spaced four multi-frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions.
Continuous	Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 48 ms to 1 s, with a resolution of 1 ms.
Set to Value	Set to a new location with or without the NDF being set. TU12 Range is from 0 to 1023 (140 – 1023 are illegal locations). TU3 Range is from 0 to 1023 (783 – 1023 are illegal locations).
TU Pointer sequences available	G.783(a) Single Alternating G.783(b) Regular + Double G.783(c) Regular + Missing G.783(d) Double Alternating G.783(e) Single G.783(f) Burst G.783(g) Periodic 87–3 G.783(g) Periodic 87–3 With Add G.783(g) Periodic 87–3 With Cancel G.783(h) Periodic G.783(h) Periodic with Add G.783(h) Periodic with Cancel Phase Transient Pointer Adjustment Burst TU-3 Periodic 85–5 TU-3 Periodic 85–5 With Add TU-3 Periodic 85–5 With Cancel TU-12 Periodic 35–1 TU-12 Periodic 35–1 With Add TU-12 Periodic 35–1 With Cancel

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
Initialization Period	On or Off Thirty second burst of 1 pointer per second in the same direction as the selected test
Cool Down Period	On or Off This will last at least 60 seconds
PDH & TU Measurements	
PDH Error Count, Error Rate and Error seconds for	Frame Bit CRC-4 (2 Mb/s only) Pattern Bit
TU Error Count, Error Rate and Error seconds for	TU12 BIP–2 TU3 BIP-2 TU12 FEBE TU3 FEBE
PDH Alarm and Failure Seconds for	AIS RAI Loss of Pattern Sync Loss of Frame Loss of Signal
TU Alarm and Failure Seconds for	TU AIS TU FERF TU Loss of Pointer TU Loss of Multiframe
TU Pointer Measurements	Seconds: Count: LOP Illegal pointers Illegal pointers Positive justifications NDF Negative justifications
G.826 Analysis for TUs	
TU12 BIP-2 & FEBE Seconds and ratio	Error Blocks, ES, SES, UAS, Background Block Errors FEBE-Count, FEBE-ES, FEBE-UAS FEBE-EFS
TU3 BIP-8 & FEBE Seconds and ratio	Error Blocks, ES, SES, UAS, Background Block Errors FEBE-Count, FEBE-ES, FEBE-UAS FEBE-EFS

Table 1–7: Option 36 2 Mb/s, 34 Mb/s, 140 Mb/s, TU12, TU3 Capabilities (Cont.)

Characteristic	Description
G.821 Analysis for PDH	
PDH Frame & CRC-4 Errors, Seconds, and % of total time	Error-Count, ES, SES, UAS, EFS, DM
Payload (Pattern Bit Errors), Seconds and % of total time	Error-Count, ES, SES, UAS, EFS, DM
M.2100 Analysis for PDH	
In Service Seconds and % of total time	Error-Count, ES, SES, UAS, EFS
Out of Service Seconds and % of total time	Error-Count, ES, SES, UAS, EFS
Jitter and Wander Analysis	Refer to *Jitter and Wander Analysis* on page 1–23
LEDs	
Status Indicators	TU AIS TU FERF TU12 BIP-2 ERROR TU3 BIP-8 ERROR PDH AIS PDH RAI PDH ERROR
Histograms for PDH & TU	
Error Count, Bit Error Rate, and Errored Seconds	PDH-Frame, 2 Mb/s CRC-4, TU-BIP, TU-FEBE, Pattern Bit
Alarms & Failures On/Off	LOS, LOF, PDH-AIS, PDH-RAI, TU-LOP, TU-AIS, TU-FERF, TU-LOM, Pattern Loss, Loss of Power
TU Pointers	TU Pointer Value, Pointer Justification
Measurement Utilities	
Measurement Control	Manual Start/Stop Timed: 1 s to 99 days with 1 s resolution Continuous
Histogram Display Resolution	Normal: 1 min, 5 min, 15 min, 1 hour (displays 72 hours with 1 min resolution) Low: 15 mins, 60 mins, 4 hrs, 12 hrs (displays 45 days with 15 min resolution)
Result Logging	All measurements are recorded with start, stop time and date. The current and previous results are stored in memory both totalized and graphical. Both graphical and totalized results can be stored on a disk.

Table 1–8: Environmental Specifications

Characteristic	Description	
Temperature	Operating:	0° C to +40° C
	Nonoperating:	–40° C to +75° C
Altitude	Operating:	4,572 m (15,000 ft)
	Nonoperating:	12,192 m (40,000 ft)
Humidity	Operating:	To 95%, relative humidity at or below +40° C for 2 hours or less
		To 90% relative humidity at or below 30° C, continuous
Transportation Handling	Qualifies under National Safe Transit Association 1s Pre-shipment Test; 1A-B-1.	

Table 1–9: Physical Characteristics

Characteristic	Description
Dimensions	Height: 165 mm (6.5 in) 191 mm (7.5 in) with accessory pouch Width: 362 mm (14.25 in) Depth: 490 mm (19.25 in) with front cover 564 mm (22.2 in) with handle extended
Weight	Net: Approximately 8.7 kg (19.3 lb) Shipping: Approximately 14.1 kg (31 lb)
Power Requirements	*Line Voltage* / *Line Frequency* 90 V to 132 V / 50/60 Hz 180 V to 250 V / 50/60 Hz 100 V to 132 V / 400 Hz Maximum current is 6 A_{RMS}.

Table 1–10: Certifications and compliances

Characteristic	Description
EC Declaration of Conformity – EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: EN 55011 Class A Radiated and Conducted Emissions [1] EN 50082-1 Immunity: IEC 801-2 Electrostatic Discharge Immunity IEC 801-3 RF Electromagnetic Field Immunity IEC 801-4 Electrical Fast Transient/Burst Immunity IEC 801-5 Power Line Surge Immunity [1] Certified with all 2 Mb/s transmit cables absent when not in use.
EC Declaration of Conformity – Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities: Low Voltage Directive 73/23/EEC EN 61010-1/A1 Safety requirements for electrical equipment for measurement, control, and laboratory use
Approvals	UL3111-1 – Standard for Electrical Measuring and Test Equipment CAN/CSA C22.2 No. 1010-1 – CSA Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use
Conditions for Safety Certification	Operating temperature: +5 to +40 °C Relative Humidity: (maximum operating) 80% up to 31 °C ,decreasing linearly to 50% at 40 °C Max. Operating altitude: 2000 m Equipment Type: Test and measuring Safety Class: Class I, grounded product (IEC1010-1) Overvoltage Category: CAT II (IEC1010-1) Polution Degree: Polution Degree 2, rated for indoor use only (IEC1010-1)

Table 1–10: Certifications and compliances (Cont.)

Characteristic	Description
Installation Category Descriptions	Terminals on this product may have different installation category designations. The installation categories are: CAT III Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location CAT II Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected CAT I Secondary (signal level) or battery operated circuits of electronic equipment

Installation

This section provides important information about installing the CTS 700-Series Test Set.

Supplying Operating Power

WARNING. *Read all information and heed all warnings in this subsection before connecting the CTS to a power source.*

AC POWER SOURCE AND CONNECTION. The CTS operates from a single-phase power source. It has a three-wire power cord and a two-pole, three-terminal grounding type plug. Make sure that the correct plug is attached to the CTS before connecting to a power source. The voltage to ground (earth) from either pole of the power source must not exceed the maximum rated operating voltage, 250 V_{RMS}.

GROUNDING. This instrument is safety Class 1 equipment (IEC designation). All accessible conductive parts are directly connected through the grounding conductor of the power cord to the grounded (earthing) contact of the power plug.

The power input plug must be inserted only in a mating receptacle with a grounding contact where earth ground has been verified by a qualified service person. Do not defeat the grounding connection. Any interruption of the grounding connection can create an electric shock hazard.

For electric shock protection, the grounding connection must be made before making connection to the instrument's input or output terminals.

Power Cord Information

A power cord with appropriate plug configuration is supplied with each CTS. Table 2–1 gives the color-coding of the conductors in the power cord. If you require a power cord other than the one supplied, refer to Table 2–2, *Power Cord Options*.

Table 2–1: Power Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral)	Light Blue	White
Grounded (Earthing)	Green/Yellow	Green

Table 2–2: Power Cord Options

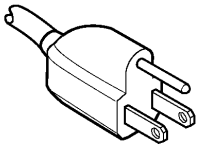
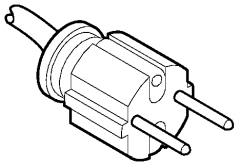
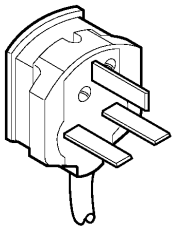
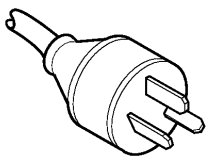
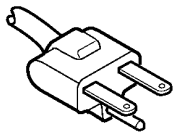
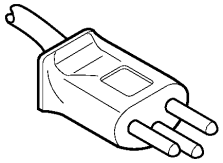
Plug Configuration	Normal Usage	Option Number	Part Number
	North America 115 V	Standard	161-0066-00
	Europe 230 V	A1	161-0066-09
	United Kingdom 230 V	A2	161-0066-10
	Australia 230 V	A3	161-0066-11

Table 2–2: Power Cord Options (Cont.)

Plug Configuration	Normal Usage	Option Number	Part Number
	North America 230 V	A4	161-0066-12
	Switzerland 230 V	A5	161-0154-00

Operating Voltage

The *Specification* section lists line voltage ranges and their associated line frequency ranges over which the CTS operates. See the *Power Requirements* specification on page 1–15 for these ranges.

CAUTION. *Before stepping the source line voltage from one range to a higher range, set the principal power switch (rear panel) to its OFF position. Failure to do so can damage the CTS.*

Your CTS is equipped with one of two possible fuse types. Either type can be used throughout the line voltage and frequency ranges. These two fuses are not totally interchangeable because each requires a different fuse cap. The fuses and their caps are listed by part number in the section *Mechanical Parts List.*

Memory Backup Power

Replaceable lithium batteries maintain internal memory modules to allow the CTS to retain the following data if you lose AC power: stored adjustment constants, saved setups, the current setup (instrument status), and test results from the last two tests.

These batteries have a shelf life of about five years. Partial or total loss of stored setups at power-on may indicate that the batteries need to be replaced.

Operating Environment

The following information describes environmental characteristics required for proper operation and long instrument life.

Operating Temperature

The CTS 700-Series Test Sets can be operated (without disk media) where the ambient air temperature is between –5° C and +40° C and can be stored (without disk media) in ambient temperatures from –40° C to +75° C. After storage at temperatures outside the operating limits, allow the chassis to stabilize at a safe operating temperature before applying power.

Ventilation Requirements

The CTS is cooled by air drawn in and exhausted through its cabinet side panels by an internal fan. To ensure proper cooling of the instrument, allow at least two inches clearance on both sides and $^3/_4$ inch on the bottom of the CTS. (The feet on the bottom of the CTS provide the required clearance when set on flat surfaces.) The top of the CTS does not require ventilation clearance.

CAUTION. *If air flow is restricted, the CTS power supply may temporarily shut down.*

Applying and Interrupting Power

Consider the following information when you power on or power off the instrument, or when power is interrupted due to an external power failure.

Powering On

At power-on, the CTS runs its power-on self test. If it passes, the CTS displays the message Internal diagnostics passed. If it fails, the CTS displays the message Internal diagnostics failed. See the *Maintenance* section for information on diagnostics and fault isolation.

Powering Off

Wait for the CTS to finish saving setups, pass/fail tests, or test results before turning off power. In general, do not power off the CTS during operations that involve saving data. If power is interrupted during a save operation, the saved data may be incomplete or corrupted.

Installed Options

The CTS may be equipped with one or more instrument options. These options are listed in the *Options* section. For further information and prices of CTS options and accessories, see your Tektronix Products catalog or contact your Tektronix Field Office.

Operating Information

This section provides an overview of CTS operation, but covers only the features needed to service or verify performance of the CTS. For more details about CTS operation, refer to the *CTS 710 SONET Test Set User Manual* or *CTS 750 SDH Test Set User Manual*.

Front-Panel Controls and Indicators

The CTS front-panel user interface consists of three major elements:

- A CRT display and the buttons around it (see Figure 2–1) display detailed test results and control most functions of the CTS.
- The buttons and the knob (see Figure 2–2) operate with the display to select menus and parameters. A few buttons control CTS functions directly.
- The status lights (see Figure 2–2) provide information at a glance about the status of the received signal.

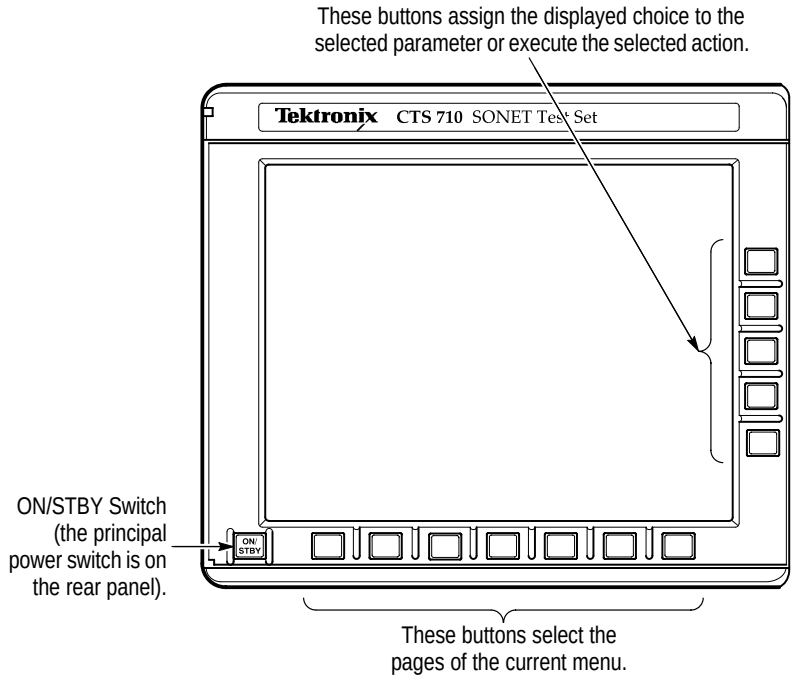


Figure 2–1: Controls Located Around the Display (CTS 710 Shown)

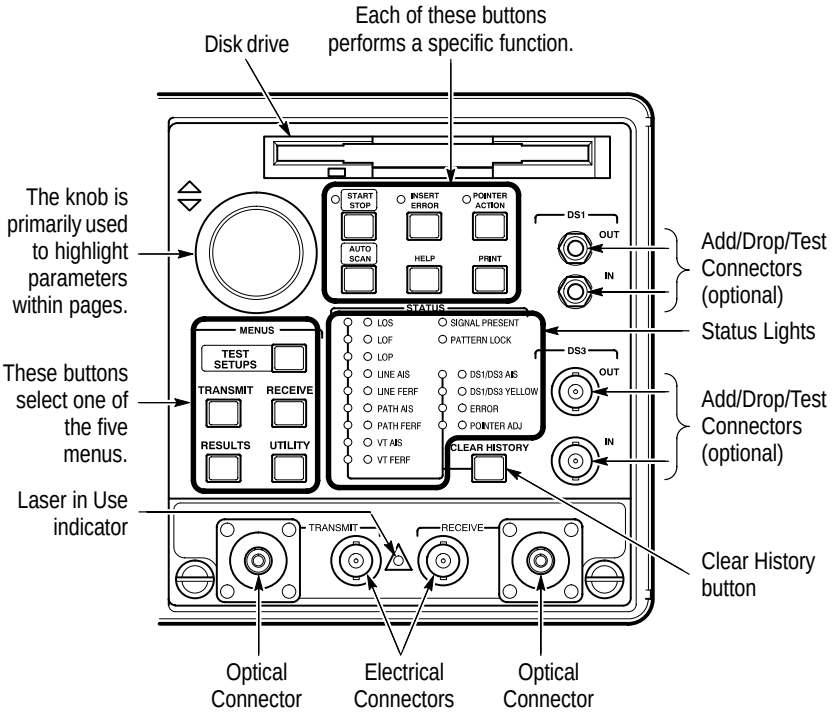


Figure 2–2: Front-Panel Controls and Indicators (CTS 710 with Option 22 Shown)

In addition to controls and indicators, the front panel contains input and output connectors for the communication signals and a disk drive for setup, test, and results storage.

Rear-Panel Controls and Connections

Figure 2–3 shows the controls and connectors on the CTS rear panel.

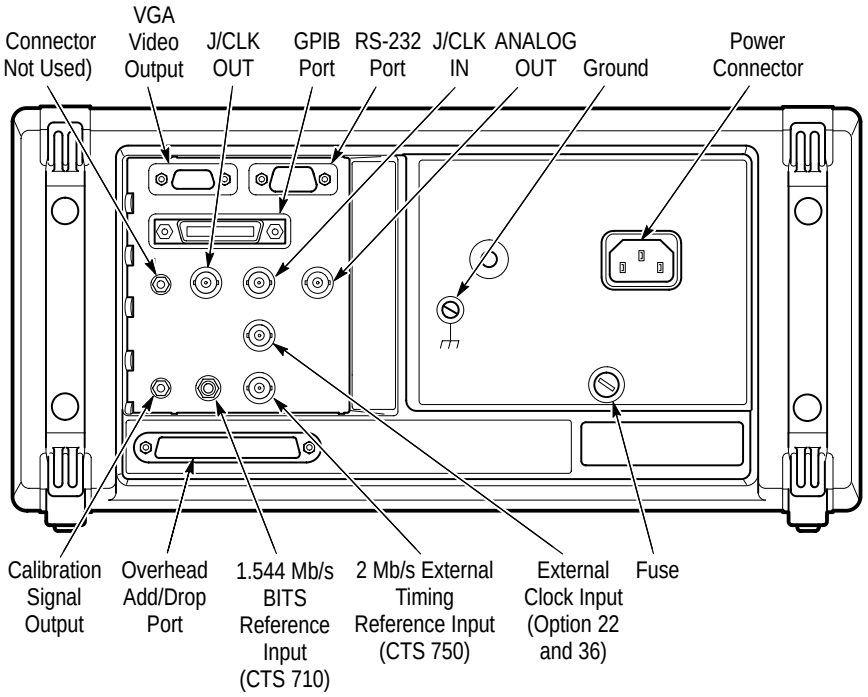


Figure 2–3: Rear-Panel Controls and Connections (CST 750 with Option 14 shown)

Front-Panel Status Lights

The status lights indicate the condition of the received signal (see Figure 2–4). There are three types of front-panel status lights:

- Green status lights. A single green light indicates that a signal is present; the second green light indicates that the CTS has achieved pattern lock on the incoming data stream.
- Red error lights. When a red error light is on, it means that the indicated error is occurring. When the red light is off, no error is occurring.
- Yellow history lights. Once an error has been detected, a yellow history light is turned on. The yellow history light shows that the associated error occurred at some time in the past. Yellow history lights remain on until you reset the error history by pressing the CLEAR HISTORY button, start a new test, or change the Receive Rate.

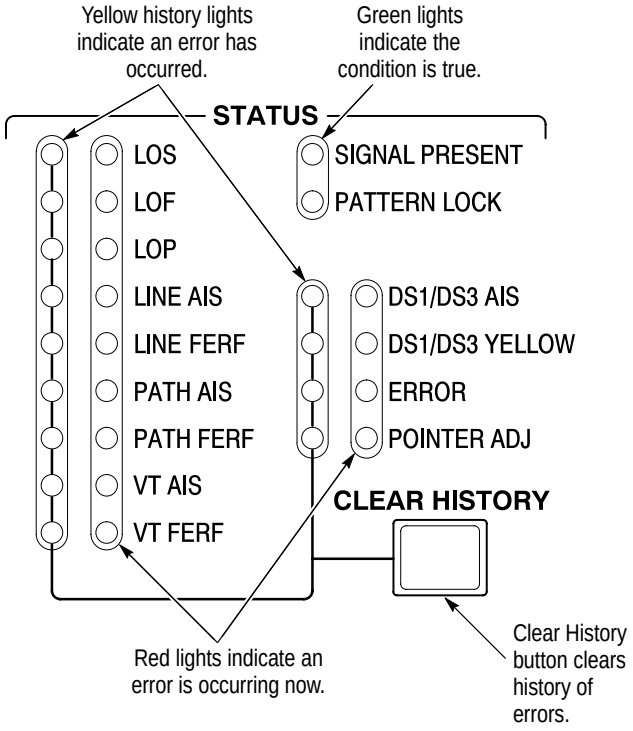


Figure 2–4: Status Lights (CTS 710 with Option 22 Shown)

Using the Menu System

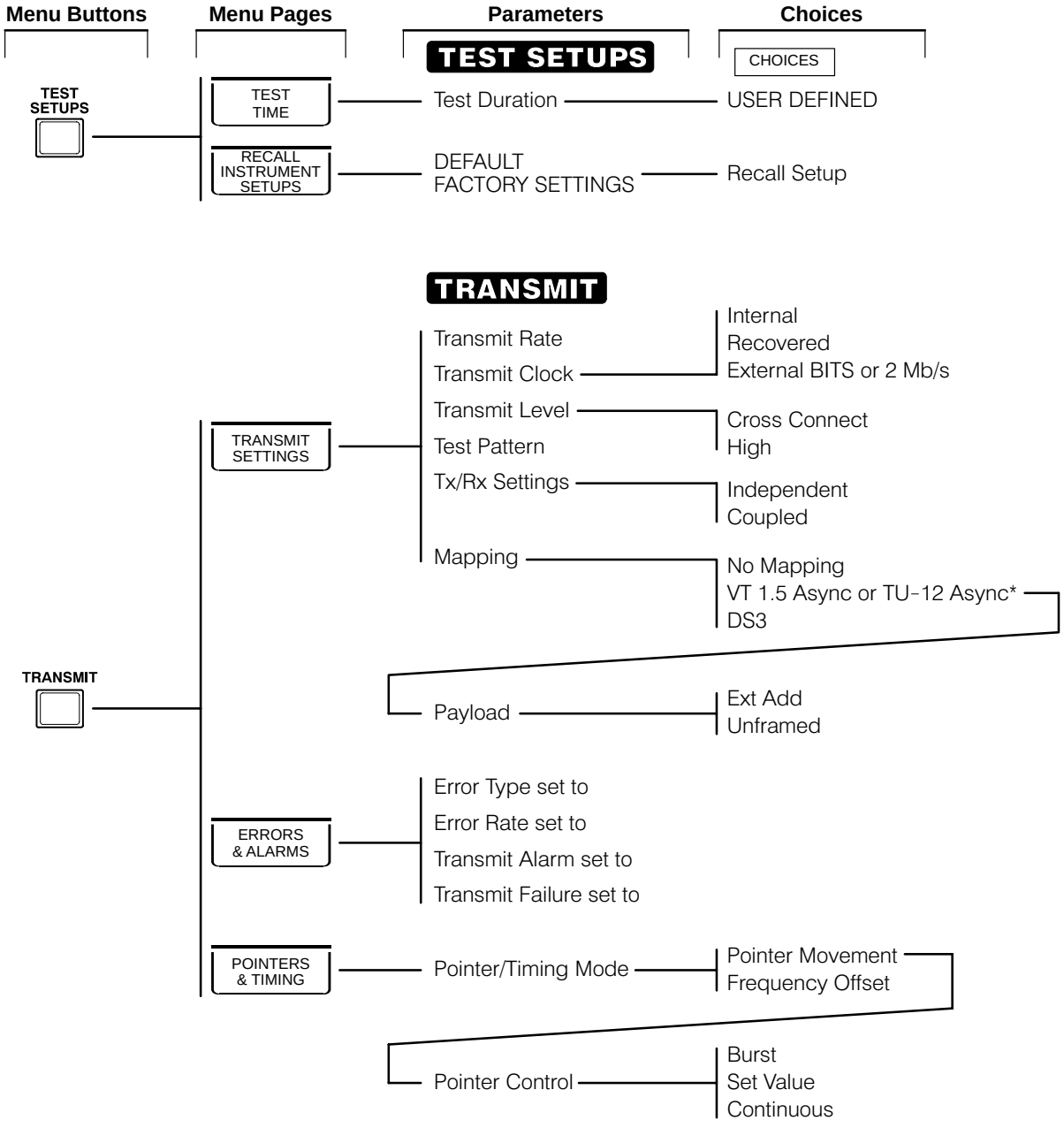
The CTS is controlled primarily by its menu system. Though several controls are located on the front panel, such as INSERT ERROR and PRINT, most functions are controlled from one of the five menus.

Operations using the menus normally consist of the following four steps. All service and performance verification procedures in this manual contain specific setup instructions to guide you through these steps.

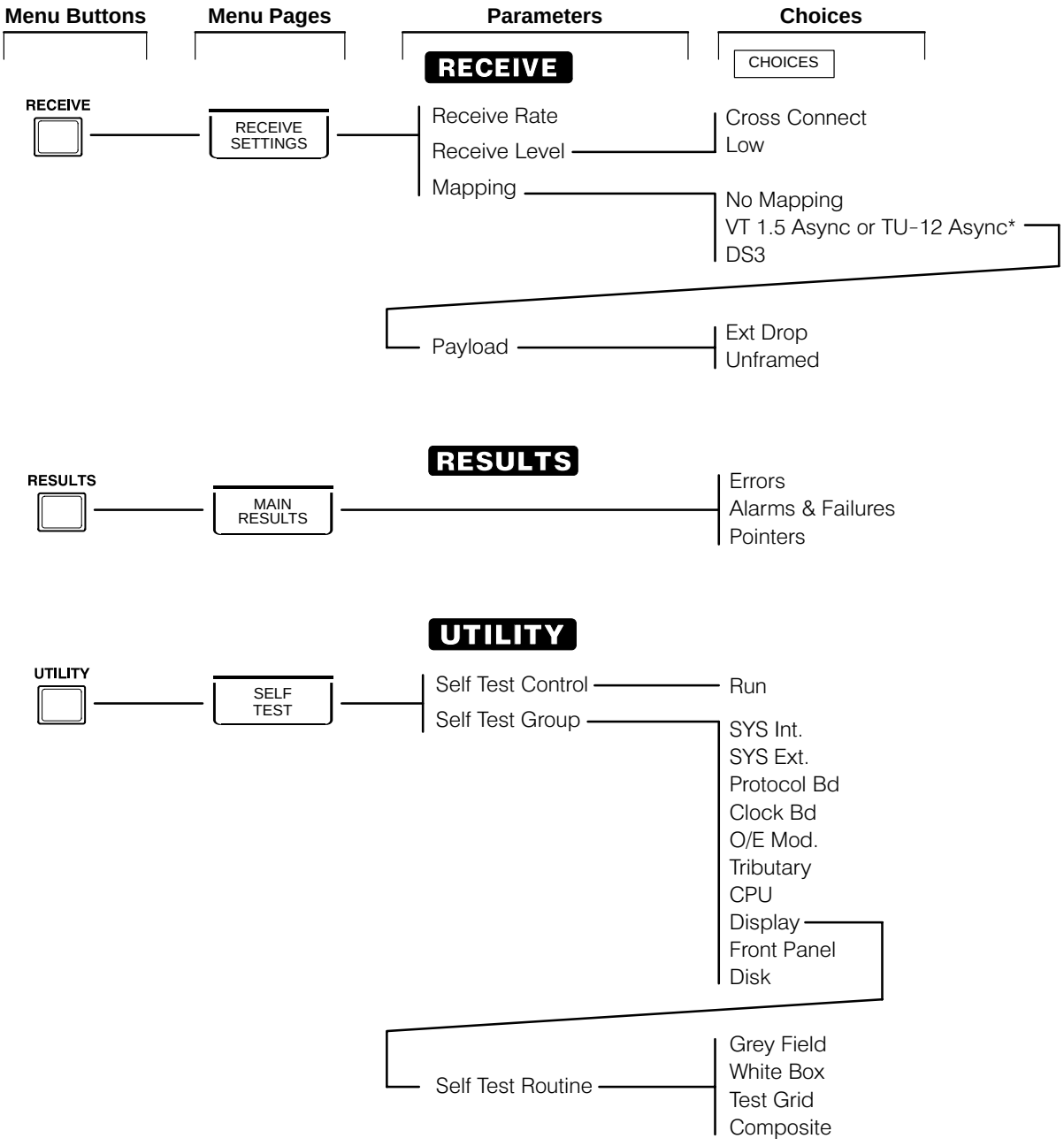
1. Press one of the five **MENU** buttons to select a menu for the display. The menus are groups of related functions, such as TRANSMIT or RECEIVE.
2. Select a menu page with one of the buttons below the display. Each menu has several pages to choose from.
3. Use the knob to highlight the parameter you want to change.
4. Use the buttons at the right side of the display to make a choice. Some choices may cause additional parameters to be displayed.

Menu Maps

The following menu maps show the menus, menu pages, parameters, and choices needed to service or verify performance of the CTS. For simplicity, many menu items not needed for service have been omitted from these diagrams.



*(Some choices cause additional parameters to become available for selection.)



*(Some choices cause additional parameters to become available for selection.)

Theory of Operation

This section describes the electrical operation of the CTS 700-Series Test Set. The description is based on the block diagram located in the *Diagrams* section of this manual, and gives an overall view of the module design. This description, together with the troubleshooting and diagnostics information in the *Maintenance* section, enable a qualified technician with the appropriate test equipment to isolate a problem to the faulty module.

Module Descriptions

As you read the following module descriptions, refer to the block diagram located in the *Diagrams* section.

A01 Display

This board contains the video display interface, a disk drive interface, non-volatile RAM, and an interface to the Protocol boards.

The video display is standard VGA format. The A01 Display circuitry sends the text and graphics information to the A26 Monitor assembly as a video signal. (Text and graphics are processed by different parts of the A01 Display circuitry.) The A01 Display circuitry also generates and sends vertical (VSYNC) and horizontal (HSYNC) sync signals to the A26 Monitor assembly. A VGA-compatible video output is available at the rear of the instrument.

The disk drive interface connects to the DOS-format floppy disk drive. All disk controller circuitry resides on the A01 Display board.

The non-volatile RAM is 256K bytes of battery-backed RAM, which is used to store setup information.

The protocol board interface circuitry passes System Bus signals to the Protocol boards. Access to the protocol boards and the interface boards passes through the A01 Display board.

A02 Backplane

The A02 Backplane is the major wiring harness and power distribution point for the CTS. The A02 Backplane regulates the ±12 V supply, and provides it to boards plugged into the A02 Backplane. For the Protocol boards, the A02 Backplane supplies ±12 V through the cable harness, not the backplane.

Regulation for –5 V is done locally on boards requiring that voltage, rather than on the A02 Backplane.

A03 CPU

The A03 CPU coordinates all CTS activities (including the activities of the Front Panel Processor). The CPU is a 16 MHz 68020 which is interfaced to a PC-AT bus for communications with peripherals. The CPU also supports the I^2C bus for serial communications to peripherals. The CPU has 1 Mb dynamic RAM and 3 Mb of FLASH EPROM program storage. A clock/calendar is also included.

A04/A05 Plug-In Interface Module

The primary function of the Plug-In Interface Module is converting the optical and electrical standard signals to (and from) the TTL and ECL digital signals used by the Protocol Processor. Secondary functions are clock recovery for the 52 Mb/s rate and measuring received optical and electrical signal levels. The optical and electrical signal levels are returned as analog voltages. The Plug-In Interface Module also has an Active Signal Present line which is polled by the CPU.

Figure 3–1 is a block diagram of the Plug-In Interface Module. The following descriptions correspond to the functional blocks shown in the block diagram.

CPU Interface. The A03 CPU board communicates with the Plug-In Interface Module through three I^2C Bus registers (1-to-8 serial-to-parallel bus expanders). These registers, called the state setup registers, are responsible for the following functions:

- Register0 is read-only and contains the board configuration, board version, and status of the Active Signal Present line.
- Register1 is read/write and controls the SONET/SDH signal interface and signal path.
- Register2 is read/write and controls the optical signal interface.

Receiver Rate Select. The Receiver Rate Select block controls the received signal path from the front-panel connectors to the protocol interface connector. The Receiver Rate Select block is controlled through the state setup registers.

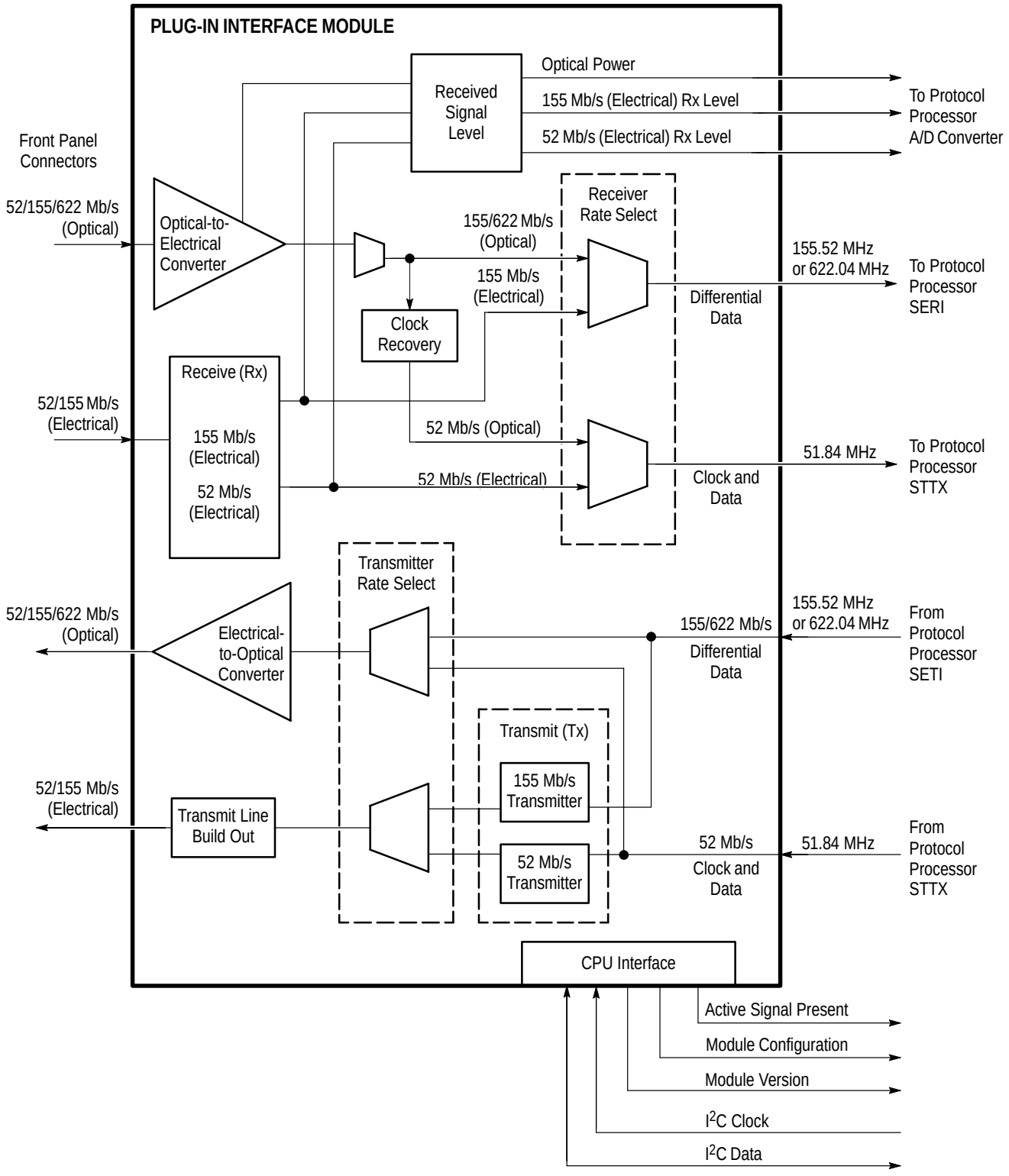


Figure 3–1: Plug-In Interface Module Functional Block Diagram

Receive (Rx). The Receive block contains the 52 Mb/s and 155 Mb/s receivers. This block also contains circuitry for detection of Active Signal Present.

The 52 Mb/s receiver performs amplification, equalization, clock recovery, data retiming, and B3ZS decoding. Note that equalization of frequency loss from the transmission cable is not automatic; it must be selected by the operator. The choices are cross-connect or low (maximum cable length). There is significant overlap in the response of the associated filters.

The 155 Mb/s receiver performs equalization and ECL conversion. No operator selections are necessary to set up the 155 Mb/s receiver. Equalization is automatic, performed by an active device.

Optical-to-Electrical Converter and Clock Recovery. The Optical-to-Electrical Converter block receives an optical signal and generates a corresponding differential ECL NRZ pulse train. It can receive 52 Mb/s, 155 Mb/s, and 622 Mb/s signal rates. The received 52 Mb/s signal undergoes further processing in the Clock Recovery block, making the signal compatible with the 52 Mb/s recovered signal format. The Clock Recovery block accepts the differential data stream and outputs a differential clock and retimed data streams, which are then level shifted to TTL levels.

Received Signal Level. Each of the receiver circuits has a peak voltage indicator or, in the case of optical signals, an average incoming power indicator.

Transmitter Rate Select. The Transmitter Rate Select block is controlled by means of the state setup registers (refer to page 3–2). This block controls the transmit signal path from the front connectors to the protocol interface connector.

This includes two groups of switches; relays to switch the outgoing analog signals, and multiplexers to switch digital data from the protocol board. The relay selects routing for the outgoing signal (to the 155 Mb/s transmitter or the 52 Mb/s transmitter), while the multiplexers select between the electrical and optical data options for the different clock rates.

Transmit (Tx). The Transmit block contains the 52 Mb/s and the 155 Mb/s transmitters.

The 52 Mb/s transmitter performs B3ZS encoding, amplification, and pulse shaping. The amplification must be selected by the operator. The choices are high or cross-connect.

The 155 Mb/s transmitter is more complicated. It has an active current source, a differential amplifier, and an all-pass network to allow matched termination at high and cross-connect outputs.

Transmit Line Build Out (LBO). The Line Build Out (LBO) feature allows the transmitter output to be degraded to approximate the defined signal at the cross-connect point (STSX-n). When LBO is not enabled, the transmitter output is unfiltered (STS-n), but will meet the Bellcore 253 specifications at the downstream cross-connect point. When LBO is enabled, the output signal conforms to Bellcore 253 specifications without any further filtering.

Electrical-to-Optical Converter. The Electrical-to-Optical Converter is a self-contained module that converts NRZ ECL differential signals (52 Mb/s, 155 Mb/s, and 622 Mb/s) to optical output.

The Electrical-to-Optical Converter also monitors the laser bias point for end-of-life, excess heat, or low bias conditions. The normal operating range of this voltage is between 0.010 V and 0.650 V, while end of useful life is indicated by a bias voltage of greater than 0.650 V.

A06 Front Panel

While the A03 CPU processor system controls CTS main function, the A06 Front Panel has its own dedicated processor. The A03 CPU processor system sends instructions to and receives information from the Front Panel Processor on the A06 Front Panel board. The Front Panel Processor monitors the settings of the front-panel switches and knob (potentiometer). Any changes in their settings are reported to the processor system. The Front Panel Processor also controls the front-panel LEDs and generates the beeper signal.

Front Panel Processor. The Front Panel Processor system consists of a single-chip microprocessor with built-in RAM, ROM, A/D converter (for digitizing the potentiometer wiper voltages), a programmable timer (for generating the outputs for the beeper), and a serial communications interface (for data transfer to and from the A03 CPU processor).

Front Panel Controls. All of the front panel controls are “soft” controls in that they are not connected directly into the signal path. The analog output levels of the front-panel knobs/potentiometers are converted to digital equivalents. Therefore, associated circuits are not influenced by the physical parameters of the controls (such as capacitance, resistance, and inductance). Buttons that are pressed are interpreted by the main CPU which converts the identification numbers reported by the Front Panel Processor into the logical functions each button represents. This mapping may be dynamic and depends upon the current operational state of the instrument. For instance, the bezel buttons located underneath and to the right of the display have a logical function which corresponds only to the current menu which is displayed.

There is no correlation between the absolute potentiometer voltage and a knob setting in the main CPU. This is due to the fact that only change information is sent from the Front Panel Processor to the main CPU.

***NOTE**. The ON/STBY switch is not read by the Front Panel Processor. The signal passes through the A06 Front Panel board, is processed by the A03 CPU board, and is passed through the A02 Backplane board to the low voltage power supply.*

Communication. A Dual Asynchronous Receive/Transmit (DUART) integrated circuit on the A03 CPU board controls and synchronizes data transfers between the main CPU and the Front Panel Processor. Data transfers between the two processors are initiated by one processor putting data into the DUART, which causes an interrupt to the other processor.

When the power is turned on, the main CPU configures the Front Panel Processor, providing specific information about the front panel controls. The Front Panel Processor needs this information to report changes correctly and to generate the proper outputs for the beeper. Once the Front Panel Processor has been configured, the main CPU goes on with other functions.

A07 Auxiliary Power

The A07 Auxiliary Power board brings the AC power into the CTS. The A07 Auxiliary Power circuitry includes the principal power switch, fuse, and line filter. It also distributes power to the monitor and fan.

A08 Clock Generator

The A08 Clock Generator generates the various clock rates needed by the Protocol boards and Tributary options. The primary purpose of the A08 Clock Generator is to provide a timing source for the transmitter. The A08 Clock Generator also generates the user-selectable clock offsets used to simulate the line frequency offset, payload frequency offset, or tributary rate offset. These offsets can also be configured to provide pointer movements (either STS, VT, or TU pointers).

The A08 Clock Generator must select a reference source for the transmit rate. The reference source can be an internal oscillator, the received line clock, or the external BITS or 2 Mb/s clock references, described below. These clock sources are fed through a multiplexer; selection is controlled by CPU interface circuitry on the A08 Clock Generator board. The clock sources then go through a phase-locked loop to generate a 51.84 MHz reference, which goes back to the Protocol Processor as reference for the transmitter.

The reference sources for the A08 Clock Generator follow:

Internal Oscillator. This crystal oscillator is a Stratum 3-level time base used as the internal reference.

Received Line Clock for Loop Timing. This signal can originate on either the Plug-In Interface Module or the A10 High Speed Protocol board, depending on

the signal rate. A 52 Mb clock signal is recovered on the Plug-In Interface Module; all other rates are recovered on the A10 High Speed Protocol board.

External BITS Reference or External 2 Mb/s Reference. Input is through a rear-panel jack. The input signal goes through a jitter reduction circuit before being fed to the multiplexer.

Any of these reference sources can be offset by means of a synthesizer on the A08 Clock Generator board.

Protocol Processor

Functionally, the A09 Main Protocol board and the A10 High Speed Protocol board can be considered a single unit, the Protocol Processor. The Protocol Processor is responsible for all generation, acquisition and manipulation of the transport overhead (TOH). If no Tributary option is present, the Protocol Processor also controls the generation and acquisition of the path overhead (POH) and payload.

The Tx part of the Protocol Processor takes data (the data is either internally generated or comes from the option boards via the Com Bus), attaches user-specified POH and TOH values, develops the user-specified multiplex structure, and converts this SONET/SDH-compatible parallel data stream to serial format. This serial data stream then goes to the Plug-In Interface Module for final line conditioning and transmission.

The Rx part of the Protocol Processor accepts data from the Plug-In Interface Module, verifies the TOH, demultiplexes the SONET/SDH stream, verifies the POH of the demultiplexed stream, and delivers this data stream to the Com Bus interface for use by options. The Protocol Processor can also take the demultiplexed data and verify the content of the payload.

The Protocol Processor also generates the Tx rate clocks needed for the specified Tx rate. The specified Tx rate is developed from the timing clock received from the A08 Clock Generator. The Protocol Processor also develops the Tx clock needed by any Tributary boards that are installed.

The functional split between the A09 Main Protocol board and the A10 High Speed Protocol board is listed in Tables 3–1 and 3–2.

Table 3–1: A09 Main Protocol Board Hardware Function Assignments

A09 Main Protocol Board Elements	Description
PTX	POH content, alarms and pointer movements, internally generated payloads
PRX	POH acquisition and alarm status, pointer movement counters, and SPE PRBS error counters
HWT	Hardware Timer, controls error and pointer insertion rates
DCC Control	Data communications channel control (section DCC and line DCC)
Com Bus Interface	Primary internal interface for passing SONET/SDH data to the option boards
Processor Interface	Control register and decode logic
FLASH EPROM	Holds the configuration data for the various XILINX FPGAs used on the board; the main CPU can program the FLASH EPROM contents

Table 3–2: A10 High Speed Protocol Board Hardware Function Assignments

A10 High Speed Protocol Board Elements	Description
SETI	For 155 Mb/s and 622 Mb/s only, parallel-to-serial conversion, CMI encoding/decoding, transmit line clock generation for 155 Mb/s and 622 Mb/s
SERI	For 155 Mb/s and 622 Mb/s only, serial-to-parallel conversion and clock recovery
STTX	SONET section DCC and F1 insertion; LOS and LAIS alarms; SONET line DCC insertion; Line FERF alarm; for 52 Mb/s, parallel-to-serial conversion
ITX	TOH, Tx multiplex structure, inactive channel content, and active channel selection
IRX	TOH acquisition and active channel selection
Clock Generator	Generates the Tx rate clocks needed for the specified Tx rate

Figures 3–2 is a block diagram of the Protocol Processor.

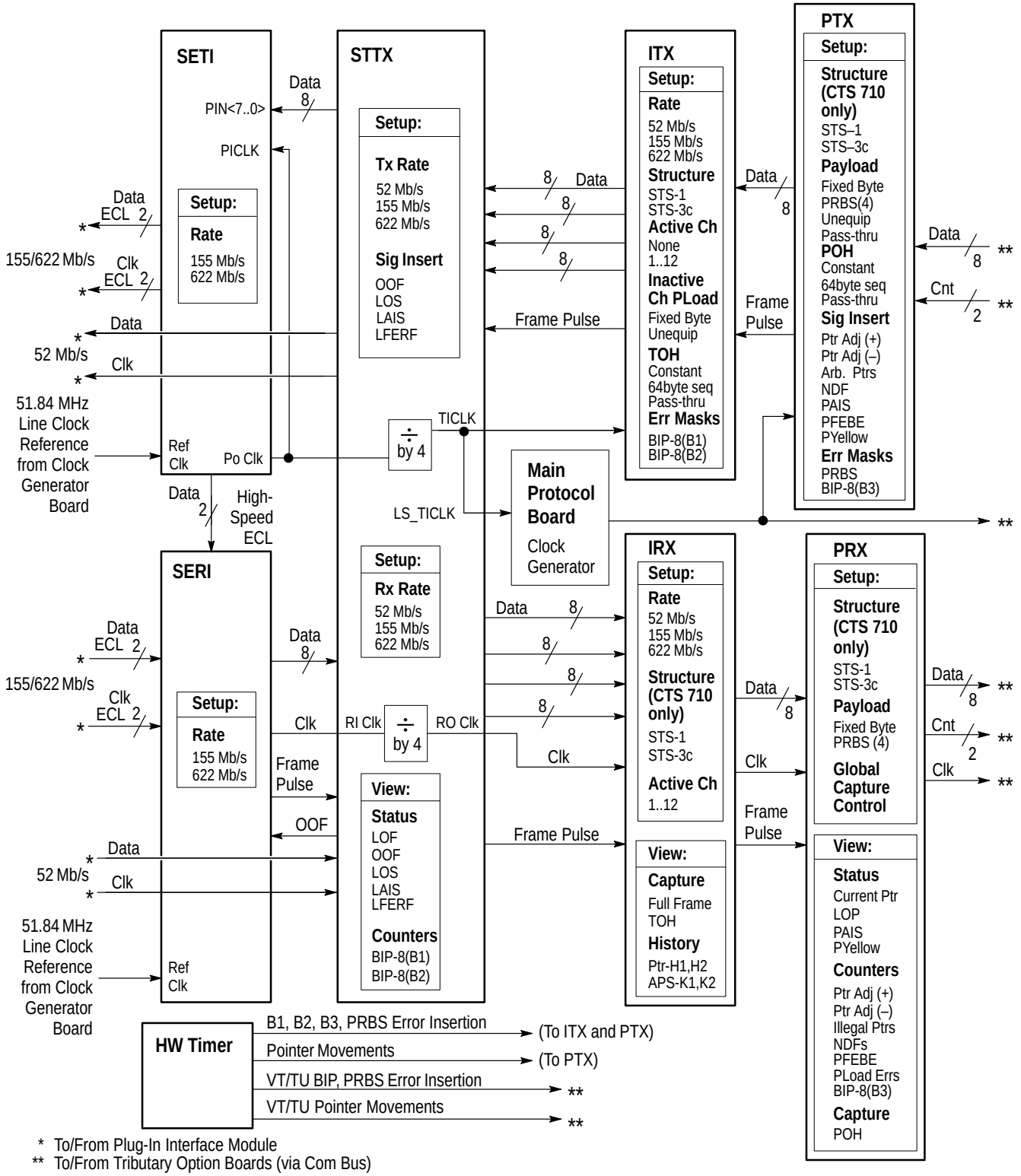


Figure 3–2: Protocol Processor Functional Block Diagram

A25 Low Voltage Power Supply

The low voltage power supply provides the +5.1 V, +15 V, –6.4 V, and –15 V supply voltages to the CTS.

The low voltage power supply is a switching power converter. It supplies power to all instrument circuitry. The low voltage power supply sends power to the A02 Backplane where it is distributed to other boards plugged into the backplane. Power is also taken directly from the power supply and sent to the Protocol boards (via a cable harness).

The POWER switch, located on the rear panel, controls all power to the instrument including the low voltage power supply. The ON/STBY switch, located on the front panel, also controls all of the power to the instrument except for part of the circuitry in the low voltage power supply.

A26 Monitor

The monitor is a raster scan cathode-ray tube (CRT) display that has 60 Hz frame and 32 kHz line rates. The CRT display circuitry is similar to that of a television monitor.

All information is displayed by the A20 CRT Driver. The driver generates the high voltages necessary to drive the CRT. It also contains the video amplifier, horizontal oscillator, and the vertical and horizontal yoke driver circuitry. The monitor gets its supply voltages from the A25 Low Voltage Power Supply through the A02 Backplane and the A07 Auxiliary Power boards. The monitor receives video signals from the A01 Display board.

Fan

The fan provides forced air cooling for the CTS. It connects to +12 V on the A02 Backplane through the A07 Auxiliary Power board.

A11/A13 Tributary Board (Option 22 and Option 36)

The Tributary board generates test signals and maps and demaps external signals into or out of the payload. The payload interface from the Tributary board to the rest of the CTS is through the Com Bus. The Tributary board is controlled by the A03 CPU via the System Bus.

The Com Bus provides a byte-wide SONET data stream with all necessary information on framing and Path Overhead location. The Tributary Test capability allows detailed processing of the SONET data stream. The Tributary board adds a Test Set to the instrument. The Test Set can map and demap tributary signals to and from the SONET stream. The test set can test the ability of the SONET stream to transport tributary signals and to determine the quality of that transmission.

The option maps and demaps internal or external tributary signals into or out of a payload. It can also function as a stand-alone test set. The SONET STS-1 payload interfaces from the option board to the rest of the CTS test set over the Com Bus. The AT bus interface on the option board is used for control of the board by the main processor in the CTS.

Figure 3–3 is a block diagram of the DS1/3 Add/Drop/Test Option.

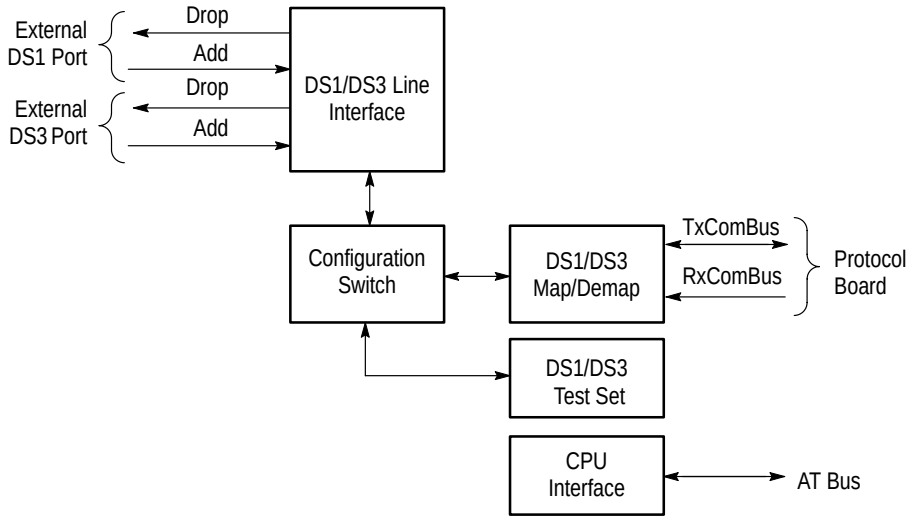


Figure 3–3: DS1/DS3 Add/Drop/Test Block Diagram

There are three independent blocks that handle the DS1 or DS3 data. They are the DS1/DS3 Line Interface, the DS1/DS3 Map/Demap, and the DS1/DS3 Test Set. These three blocks communicate through the Configuration Switch, which can connect the outputs of any of the three blocks to any combination of inputs of the three blocks. All blocks change between DS1 and DS3 modes at the same time, making it impossible to have both DS1 and DS3 modes active simultaneously in different blocks. The function of each block is described below:

- The DS1 and DS3 Line Interfaces provide the input and output physical layer interfaces as defined in ANSI T1.102-1991.
- The DS1/DS3 Mapper/Demapper maps/demaps the DS1 or DS3 signal into/out of an STS-1 payload.
- The DS1/DS3 Test Set does DS1/DS3 data generation and verification.
- The Configuration Switch interconnects the DS1/DS3 I/O of the above three blocks.
- The CPU Interface provides the CPU control of the circuit.

The processor controls the DS1/DS3 Add/Drop/Test Option over the AT bus.

A13 Tributary Board (Option 36)

Option 36 includes the circuitry discussed here and the circuitry discussed in *A11/A13 Tributary Board (Option 22 and Option 36)* on page 3–10.

The E4 circuitry is located on the daughter board portion of option 36. The E1/E3 part of option 36 is located on the mother board. No E4 signals go to or come from the mother board. However, some E1/E3 signals pass through the E4 board when the E4 board is inactive and the mother board is active. The mother board provides:

- Flash ROM that holds the Xilinx programs
- A part of the processor interface — of the address bus only 12 bits are sent to the E4 board
- Com Bus
- DC power
- Mechanical connection to the chassis
- All of its normal functions when the E4 board is inactive

The rest of this discussion deals with the E4 option as if it were an independent option. The E4 option has three major independent blocks (see Figure 3–4). These are the E4 Line Interface, the Mapper/Demapper, and the Test Set). There is a fourth minor block dealing with the External Clock Input. Each of these major blocks can input and output parallel E4 data. The output of any major block can be selected as the input for any major block, excluding looping the output of a major block back to its input. The input data path of each major block has a two to one multiplexer to select its source.

The last block, not involved in any direct tributary signal manipulation but making it all possible, is the CPU interface.

Line Interface. The E4 Line Interface converts between the voltage levels and protocols on the actual E4 serial signals (as defined in CCITT G.708) and the parallel TTL signal levels and protocols used by the Mapper/Demapper and Test Set.

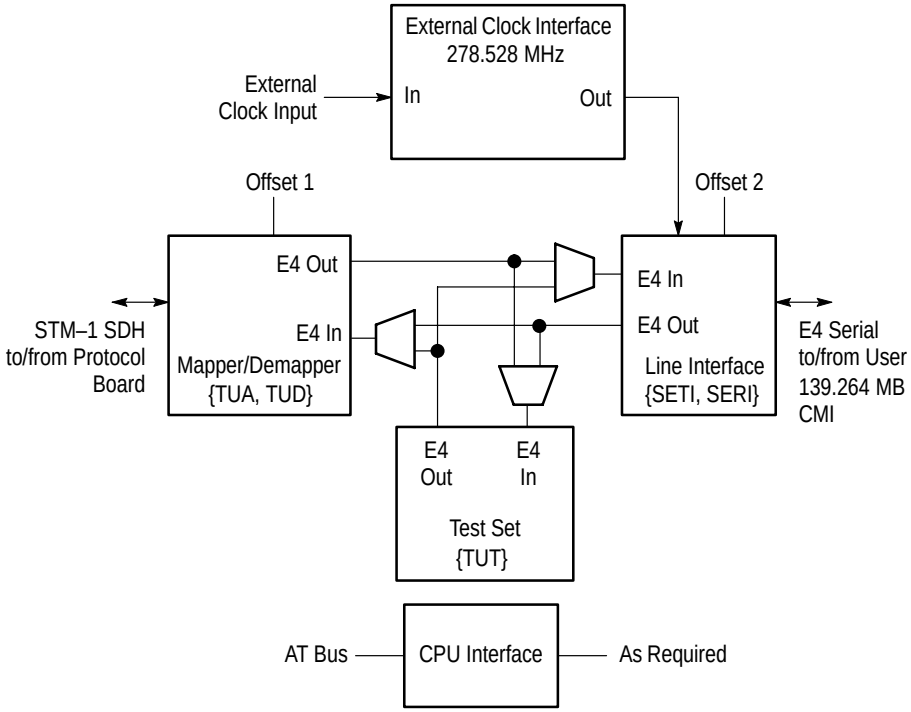


Figure 3–4: E4 Block Diagram (E1/E3 Support Functions Not Included)

Mapper/Demapper. The E4 Mapper/Demapper maps/demaps the E4 signal into/out of an STM-1 AU4 Floating Async payload. The mapping function is independent of the demapping function. Each has its own gate array that implements the required features. The TUA handles the mapping (Add) function. The TUD handles the demapping (Drop) function.

The input to the mapper can come from either the Line Interface or the Test Set. Either source will have a non-gated 17.408 MHz clock. This clock and Offset 1 (19.44 MHz) are used to decide when to carry data. This decision and the incoming E4 parallel data is put into the FIFO. This is done at the fixed nominal rate of 17.408 MHz.

The data is read out of the FIFO by a gated 19.44 MHz clock derived from the Tx Com Bus. It is read as needed by the circuit that maps the E4 data into a VC4 container. On average, the FIFO input and output data must be equal.

The input to the demapper comes from the Rx Com Bus. The demapped data can go to either (or both) the Line Interface (to become dropped data) or the Test Set.

Test Set. Basically the Test Set generates a framed or unframed E4 pattern and supplies the required errors and alarms. This signal can go to either the Tx Line Interface or the Mapper. The Test Set also receives an E4 source from either the Rx Line Interface or the demapped signal and checks for a framed or unframed pattern (as set by software) and any errors or alarms.

External Clock Interface. The E4 Transmit signal can use an externally supplied clock as its source. The frequency will be twice the bit-rate (nominally 278.528 MHz). This is fed to the SETI and divided down to the E4 byte-rate (nominally 17.408 MHz) that the rest of the generator circuits use.

CPU Interface. The CPU interface is not involved in any direct tributary signal manipulation, but makes it all possible.

The processor controls the Tributary board over the AT bus. The Tributary board uses a 14-bit address (from the mother board as well as a chip select) and a 16-bit data interface. Read-write registers control all operations of the Tributary board .

A14 JAWG Board (Option 14)

Option 14 includes the A14 JAWG (jitter and wander generator) and A12 JAWA (jitter and wander analyzer) circuitry discussed here and on page 3–16.

The JAWG board generates a clock signal that is modulated by wander or jitter at a programmed frequency and amplitude. The CTS can use the jittered clock (in place of a stable clock) to set the timing of the transmit outputs for each of the data rates. The jittered clock is also available as an output at the rear panel. Figure 3–5 shows a block diagram of the JAWG circuitry.

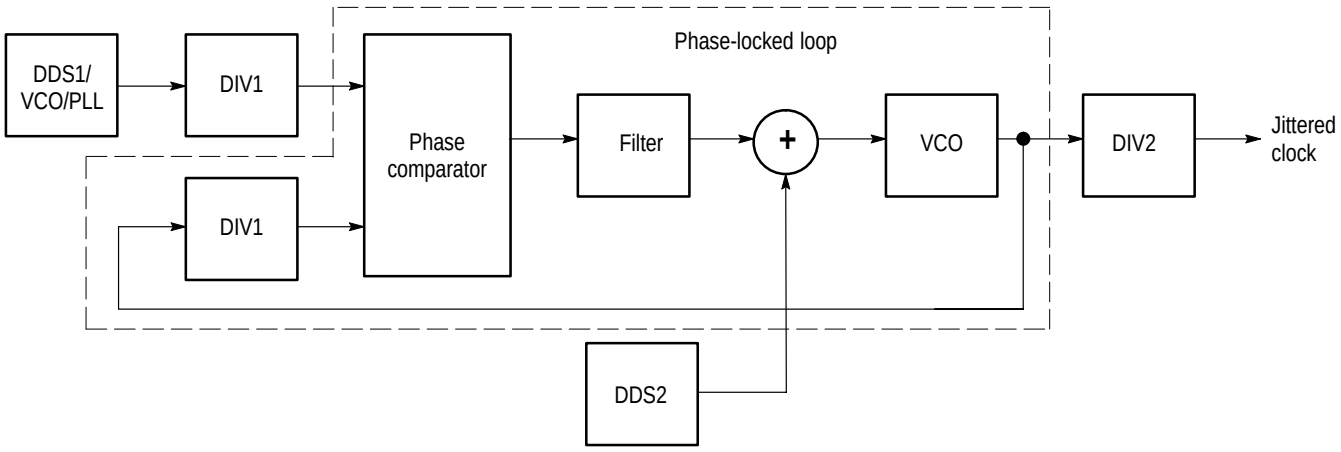


Figure 3–5: JAWG Block Diagram

DDS1/VCO/PLL. The DDS1/VCO block is an oscillator that sets the nominal clock frequency for the JAWG. Clock timing is based on direct digital synthesis (DDS) at a nominal 4.86 MHz, which is then multiplied up to the clock frequency by the voltage controlled oscillator VCO in phase-locked loop.

Wander and jitter with modulation frequencies below 1 kHz is generated directly by reprogramming the DDS1 output frequency in real time.

DIV1. There are two matching frequency dividers labeled DIV1 that set the jitter generation amplitude range. Frequency dividers are required prior to the phase comparator to generate jitter amplitudes greater than one unit interval.

DDS2. The DDS2 block generates the jitter modulation frequency using direct digital synthesis. Its output amplitude, which is programmable, determines the jitter modulation amplitude of the jittered clock.

Phase-Locked Loop. The phase comparator begins the phase-locked loop that generates the jittered clock. The filter, summer, and VCO complete the phase-locked loop.

When generating jitter with modulation frequencies above 1 kHz, the DDS1/VCO block supplies the nominal clock frequency. The summer adds the jitter frequency, which is above the loop bandwidth, to modulate the clock frequency.

DIV2. Frequency divider DIV2 divides the phase-locked loop output frequency down to the clock rate required by the CTS. The divider ratio is determined by the transmit rate setting.

A12 JAWA Board (Option 14)

The JAWA (jitter and wander analyzer) board measures peak-to-peak or RMS jitter from the received signal or from a rear-panel input. Figure 3–6 shows a block diagram of the JAWA circuitry.

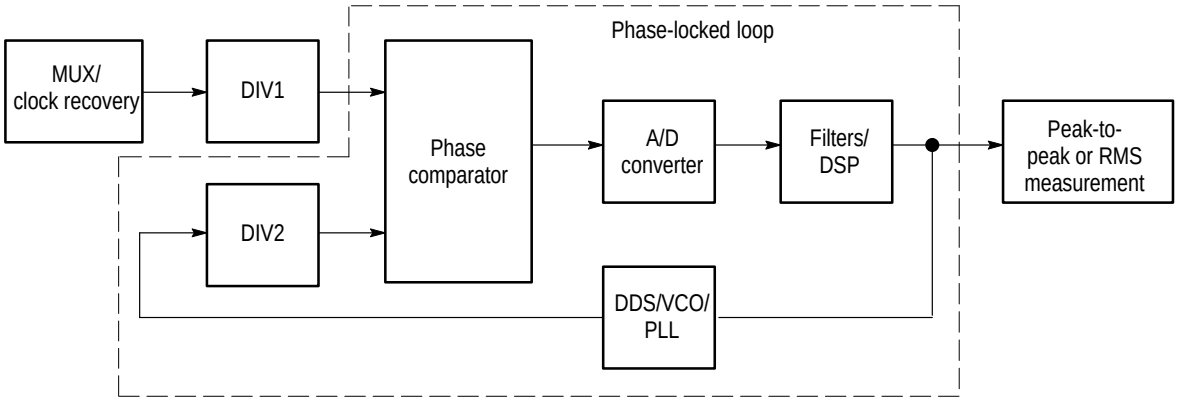


Figure 3–6: JAWA Block Diagram

MUX/Clock Recovery. The multiplexer and clock recovery block selects the source to be measured and recovers a clock from it.

DIV1. Frequency divider DIV1 divides the frequency of the source. A frequency divider is required prior to the phase comparator in order to measure jitter amplitudes greater than one unit interval.

Phase-Locked Loop. The phase-locked loop tracks the frequency of the divided input source. The loop consists of a phase comparator, an A/D converter, a digital filter and digital signal processing (DSP) block, a DDS/VCO block, and another frequency divider.

The digital filters and DSP block set programmable corner frequencies for the jitter measurement filters. The DSP function also maintains lock in the loop by controlling the output frequency of the DDS/VCO block.

The DDS/VCO/PLL block is itself a phase-locked loop. A reference frequency is generated using direct digital synthesis (DDS) under control of the DSP function. The VCO is part of a phase-locked loop that multiplies the DDS output frequency by a factor of 128.

Frequency divider DIV2 divides the VCO output frequency so that both inputs to the phase comparator are at the same nominal frequency.

Peak–to-Peak or RMS Measurement. The digital output from the DSP function contains the data necessary to calculate peak-to-peak or RMS jitter and wander in the input signal. This data is passed to the CPU to make that calculation.

Performance Verification

The performance verification procedures in this section verify the CTS 710 SONET Test Set and the CTS 750 SDH Test Set. You may only need to perform a few of these procedures, depending on what you want to accomplish. Refer to Table 4–1 to determine which procedures you need to do.

Table 4–1: CTS Performance Verification Guide

If What You Want to Accomplish is	Perform These Procedures	Approximate Time to Complete	Test Equipment Needed	Procedure Begins on Page
A quick test of the CTS without removing it from your application setup	Self Test	Five minutes	None	4–14
A more thorough test of the CTS functionality	Functional Tests	Ten minutes	75 Ω coaxial cable (standard accessory), optical fiber cable[1], optical attenuator (10 dB)[2]	4–15
A complete verification of all warranted specifications	Functional Tests Physical Layer Tests	Thirty minutes Three hours	All test equipment listed in Table 4–2	4–15 4–20
A verification of Option 22	All tests for Option 22	Two hours	Test equipment listed in Table 4–2	4–56
A verification of Option 36	All tests for Option 36	Two hours	Test equipment listed in Table 4–2	4–76
A verification of Option 14	All tests for Option 14	Three hours	Items 12, 13, 18, 19 (three required), and 27 listed in Table 4–2	4–111

1 **The optical fiber cable is only required if one of the optional Optical/Electrical Plug-In Interface Modules is installed.**

2 **The optical attenuator is only required if Option 05 is installed.**

General Information and Conventions

Please read the following general information and conventions, which apply throughout this section:

- Each test procedure begins with a table, similar to the one below, that provides information you need to know before starting the test.

Equipment Required	Communications signal analyzer (item 4) SMA male-to-BNC female adapter (item 23) Delay line (item 24), three required
Prerequisites	Prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

The item numbers after each piece of equipment refer to line numbers in Table 4–2, *Required Test Equipment*, which begins on page 4–4. The time estimates assume all the necessary equipment has been gathered, and that the equipment is warmed up and is ready to use.

- This manual presents setup instructions for the CTS in tables. Perform the steps reading from left to right in the table (see example below).

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
Begin here with Step 1	Step 2	Step 3	Step 4
		Step 5	Step 6
		Step 7	Step 8, CTS setup is complete

Menu buttons are located on the instrument front panel (see Figure 4–1). Select menu pages with the buttons below the display. Use the knob to highlight a parameter; then use the buttons at the right side to select a choice. Many setups require several iterations of highlighting parameters and selecting choices. Some setups may require more than one menu button or menu page selection as well.

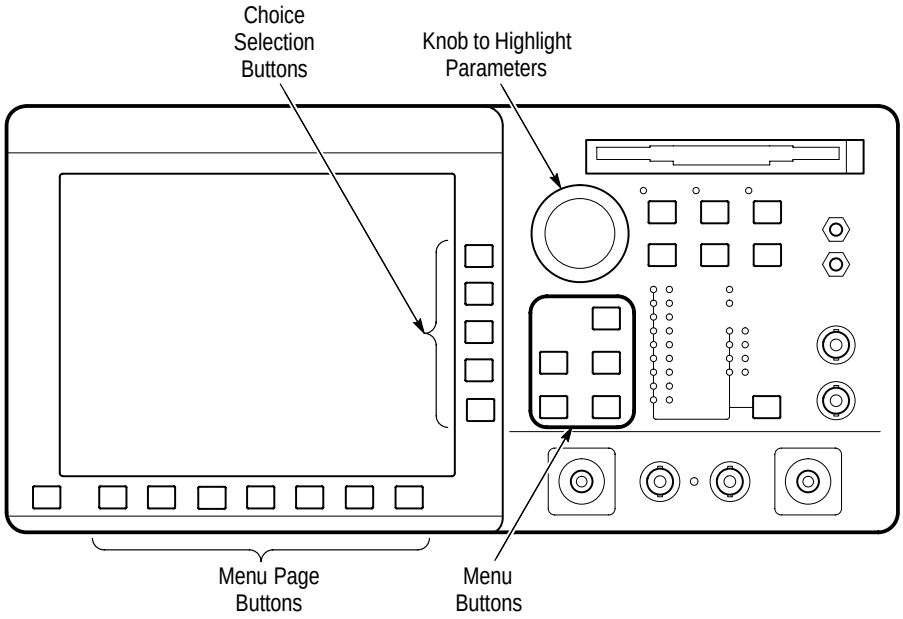


Figure 4–1: Location of Front-Panel Controls

- Most procedures mention both SONET and SDH terminology in their instructions to set the CTS controls. Please use the terminology that is appropriate to your application and disregard the other.

Equipment Required

The *Physical Layer Tests* use traceable signal sources and measurement instruments to check performance. Table 4–2 lists the required equipment. However, some specific items may not be required depending on the exact configuration of your CTS (see table footnotes).

You can obtain an accuracy ratio of 4:1 or better by using the recommended equipment listed in the *Example* column of Table 4–2. If your test equipment does not meet the minimum requirements listed in the table, your test results may be invalid.

Table 4–2: Required Test Equipment

Item Number and Description		Minimum Requirements	Example	Purpose
1	Universal Counter/Timer	160 MHz frequency measurement capability; frequency ratio B/A capability; 0.25 ppm time base accuracy; 9 digits; averaging to 10^8	Tektronix DC 5010 Digital Counter/Timer with TM 5000 mainframe[1] (if available), or an HP53131A Universal Counter with Option 001	Checking transmit clock accuracy
2	Frequency Synthesizer	750 kHz to 630 MHz frequency range; ≤ 10 Hz resolution below 30 MHz; ≤ 50 Hz resolution from 300 MHz to 320 MHz; ≤ 100 Hz resolution from 600 MHz to 630 MHz; ≤ 1 ppm frequency error; +13 dBm sine wave output into 50 Ω	Rohde & Schwarz Signal Generator SMX	Checking clocks
3	Oscilloscope	500 MHz bandwidth; 50 Ω input impedance; ≤ 1.5% DC vertical accuracy	Tektronix TDS 520B (use item 4 if item 3 is unavailable)	Checking trigger output signal
4	Communications Signal Analyzer	1 GHz bandwidth, mask testing capability with SONET masks for STS-1, STS-3, STSX-3, OC-1, OC-3, and OC-12, or SDH masks for STM-1 and STM-4	Tektronix CSA 803A Communication Signal Analyzer with SD-22 Sampling Head	Checking transmit signal shape
5	2 Mb/s Signal Source[2]	Provides 2 Mb/s signal	Tektronix CTS 750 Test Set (in addition to the CTS-under-test)	Checking 2 Mb/s Reference Input and Add/Drop/Test
6	Optical Attenuator[3]	Compatible with 62.5 µm multimode fiber; attenuation range from 0 dB to 50 dB for λ = 1310 nm, 1550 nm	Tektronix OA 5022 with TM 5000 mainframe[1]	Check receiver sensitivity
7	SONET Reference Receiver and Power Meter[4]	Calibrated frequency response for OC-1 and OC-3; 0 dBm to –80 dBm dynamic range; ≤ 5% accuracy for λ = 1310 nm, 1550 nm	Tektronix ORS156, Option 31	Check transmit signal power and shape
8	Filter	BNC connectors on each end	Tektronix FS 156 (part of ORS156)	Check pulse shape
9	SONET Reference Receiver and Power Meter[5]	Calibrated frequency response for OC-1, OC-3, and OC-12; 0 dBm to –80 dBm dynamic range; ≤ 5% accuracy for λ = 1310 nm, 1550 nm	Tektronix ORS622, Option 31 and Option 41	Check transmit signal power and shape
10	SDH Reference Receiver and Power Meter[6]	Calibrated frequency response for STM-1; 0 dBm to –80 dBm dynamic range; ≤ 5% accuracy for λ = 1310 nm, 1550 nm	Tektronix ORS156	Check transmit signal power and shape

Table 4–2: Required Test Equipment (Cont.)

Item Number and Description		Minimum Requirements	Example	Purpose
11	SDH Reference Receiver and Power Meter[7]	Calibrated frequency response for STM-1 and STM-4; 0 dBm to –80 dBm dynamic range; ≤ 5% accuracy for λ = 1310 nm, 1550 nm	Tektronix ORS622, Option 41	Check transmit signal power and shape
12	Spectrum Analyzer[8]	Frequency range 2 MHz to 1 GHz,	Tektronix 2712	Check jitter
13	Optical Fiber Cable[3] (two required)	62.5/125 µm multimode fiber; FC/PC connector on one end; compatible with CTS connector option on other end	FC/PC-to-FC/PC, Tektronix part number 174-2322-00	Interconnect optical signals
14	10 dB Optical Attenuator[9]	10 dB attenuation at λ = 1550 nm, with connectors compatible with item 13 and CTS connector option.	Tektronix part number 119-5118-00 (Included with Option 05)	Provide optical attenuation at 1550 nm
15	100 ft (31 m) length of 75 Ω Reference Cable	BNC connectors on each end	AT&T 728B reference cable	Check receiver sensitivity
16	225 ft (68.6 m) length of 75 Ω Reference Cable (two required)	BNC connectors on each end	AT&T 728B reference cable	Check receiver sensitivity
17	106 ft (33 m) length of 75 Ω Reference Cable	BNC connectors on each end	AT&T 728B reference cable	Check cable equalization
18	75 Ω-to-50 Ω Impedance Converter	Convert 75 Ω to 50 Ω impedance; 5.71 dB attenuation, BNC connectors	Min-Circuits part number BMP-5075	Interconnect electrical signals
19	75 Ω Coaxial Cable (three required)	75 Ω impedance; ≈1 m length, BNC connectors	Tektronix part number 012-1338-00	Interconnect electrical signals
20	75 Ω 10X Attenuator	75 Ω impedance; 10X (20 dB) attenuation; BNC connectors	Tektronix part number 011-0061-00	Interconnect electrical signals
21	50 Ω Power Splitter	50 Ω impedance; SMA female connectors	Tektronix part number 015-0565-00	Interconnect electrical signals
22	50 Ω SMA Coaxial Cable (two required)	50 Ω impedance; SMA male connectors	Tektronix part number 174-1364-00	Interconnect electrical signals
23	Adapter, SMA Male-to-BNC Female (three required)	50 Ω impedance	Tektronix part number 015-1018-00	Interconnect electrical signals
24	Delay Line	50 Ω impedance; SMA connectors; 15 ns ≤ delay ≤ 48 ns	Tektronix part number 015-1006-00 (5 ns each, three required) or Tektronix DL-11 Delay Line with standard accessory 174-1427-00	Delay trigger signal
25	50 Ω BNC Coaxial Cable (three required)	50 Ω impedance; BNC male connectors	Tektronix part number 012-0057-01	Interconnect electrical signals

Table 4–2: Required Test Equipment (Cont.)

Item Number and Description		Minimum Requirements	Example	Purpose
26	Adapter, BNC Female-to-BNC Female (two required)	50 Ω impedance; BNC female connectors	Tektronix part number 103-0028-00	Interconnect electrical signals
27	Adapter, Type N Male-to-BNC Female	50 Ω impedance	Tektronix part number 103-0045-00	Interconnect electrical signals
28	50 Ω SMB-to-BNC Coaxial Cable	50 Ω impedance; SMB female connector on one end, BNC male connector on the other	Tektronix P6041	Interconnect electrical signals
29	100 Ω Cable, Bantam-to-Bantam[10] (two required)	Three-conductor cable; miniature phone plug (Bantam) on each end	Tektronix part number 012-1314-00	Interconnect electrical signals
30	100 Ω Cable, Bantam-to-Bantam (two required)	Twelve inch, three-conductor cable; miniature phone plug (Bantam) on each end	Tektronix part number 012-1500-00	Interconnect electrical signals
31	Adapter Cable, Miniature Phone Plug (Bantam) to WECo 310 Plug[10]	Three-conductor cable; miniature phone plug (Bantam) on one end; WECo 310 plug on other end	ADC Telecommunications Model PJ942 Conversion Patch Cord	Interconnect electrical signals
32	Adapter, Bantam Jack-to-WECo 310 Plug[12] (two required)	Three-conductor adapter; miniature phone jack (Bantam)-to-WECo 310 plug	Tektronix part number 103-0365-00	Interconnect electrical signals
33	Tributary Signal Converter/Attenuator	Convert impedance of 100 Ω DS1 and 120 Ω 2 Mb/s tributaries to 50 Ω and attenuate by 5X	Tektronix part number 067-0250-01	Interconnect electrical signals
34	120 Ω Cable, DIN41628L Male-to-DIN41628L Male[11] (two required)	Three-conductor cable; DIN41628L (Siemens) jack on both ends	Tektronix part number 012-1469-00	Interconnect electrical signals
35	120 Ω Cable, DIN41628L Male-to-DIN41628L Male[11] (two required)	Six inch, three-conductor cable; DIN41628L (Siemens) jack on both ends	Tektronix part number 012-1501-00	Interconnect electrical signals
36	Adapter, BNC Male-to-Dual Binding Posts[10]	Binding posts on 0.75 in spacing that accept banana plugs	Tektronix part number 103-0035-00	Interconnect electrical signals
37	Adapter Cable, Bantam Plug-to-Banana Plug[10]	Tip and ring signals connected to banana plugs on 0.75 in spacing	ITT/Pomona Electronics part number 4281-36	Interconnect electrical signals
38	10X Attenuator	75 Ω impedance; 10X (20 dB) attenuation; BNC connectors	Mini-Circuits part number CAT-20-75	Interconnect electrical signals
39	2X Attenuator	75 Ω impedance; 2X (6 dB) attenuation; BNC connectors	Mini-Circuits part number CAT-6-75	Interconnect electrical signals
40	10X Attenuator	50 Ω impedance; 10X (20 dB) attenuation; BNC connectors	Tektronix part number 011-0059-02	Interconnect electrical signals
41	2X Attenuator	50 Ω impedance; 2X (6 dB) attenuation; BNC connectors	Tektronix part number 011-0069-02	Interconnect electrical signals
42	50 Ω Termination	50 Ω impedance; BNC connectors	Tektronix part number 011-0049-01	Interconnect electrical signals

Table 4–2: Required Test Equipment (Cont.)

Item Number and Description		Minimum Requirements	Example	Purpose
43	75 Ω Termination	75 Ω impedance; BNC connectors	Tektronix part number 011-0102-00	Interconnect electrical signals
44	Adapter, BNC-Male to BNC-Male	50 Ω impedance; BNC male connectors	Tektronix part number 103-0029-00	Interconnect electrical signals
45	Adapter, BNC Female to BNC-Male	75 Ω female BNC to 50 Ω male BNC	Min-Circuits part number BMP-5075R	Interconnect electrical signals

1 An additional TM 5000 mainframe is not required if one of the recommended Tektronix SDH/SONET Reference Receiver and Power Meters is used. The footnoted items can share the mainframe with the Tektronix SDH/SONET Reference Receiver and Power Meter.

2 This equipment is required to test a CTS 750. It is not required to test a CTS 710.

3 This equipment is required to test a CTS 710 or CTS 750 with any one of the optional Optical/Electrical Plug-In Interface Modules installed; otherwise, it is not required.

4 This equipment is required to test a CTS 710 with the 52/155 Mb/s Optical/Electrical Signal Interface Module installed; otherwise, it is not required.

5 This equipment is required to test a CTS 710 with the OC 1/3/12 Optical/Electrical Module installed; otherwise, it is not required.

6 This equipment is required to test a CTS 750 with the 52/155 Mb/s Optical/Electrical Signal Interface Module installed; otherwise, it is not required.

7 This equipment is required to test a CTS 750 with the OC 1/3/12 Optical/Electrical Module installed; otherwise, it is not required.

8 This equipment is required to test a CTS 750 with Option 14 only.

9 This equipment is required to test a CTS 710 or CTS 750 with Option 05 only.

10 This equipment is required to test a CTS 710. It is not required to test a CTS 750.

11 This equipment is required to test a CTS 750 with Option 36 only. It is not required to test a CTS 750 without Option 36 or a CTS 710.

12 This equipment is required to test a CTS 710 with Option 22 only. It is not required to test a CTS 710 without Option 22 or a CTS 750.

Test Record

Photocopy either Table 4–3 (for CTS 710) or Table 4–4 (for CTS 750), found on the next pages, and use it to record the performance verification results for your instrument.

Table 4–3: CTS 710 (SONET) Test Record

CTS 710 Serial Number:	Temperature and Relative Humidity:
Plug-In Interface Module Type:	Verification Performed by:
Plug-In Interface Module Serial Number:	Date of Verification:

CTS 710 Functional Tests

Test		Passed	Failed
System Self Test with External Loop-Back			
Generated Failures	None		
	LOS		
Pointer Movements	Continuous		

CTS 710 Physical Layer Tests

Transmit Output Checks		Minimum	Measured Value	Maximum
Electrical Signal Level at Transmit Output	STS-1 Cross Connect Level	680 mV		920 mV
	STS-3 High Level	720 mV		880 mV

		Passed	Failed
Electrical Output Pulse Shape	STS-1 High Level		
	STSX-1		
	STS-3 High Level		
	STSX-3		
Optical Output Pulse Shape	OC-1		
	OC-3		
	OC-12		

Receive Input Checks		**Passed**	**Failed**
Electrical Input Sensitivity	STS-1 High (part 1)		
	STS-1 High (part 2)		
	STSX-1		
	STS-1 Low		
	STS-1 Monitor		
	STS-3 High (part 1)		
	STS-3 High (part 2)		
	STSX-3		
	STS-3 Low		
	STS-3 Monitor		
Optical Input Sensitivity	OC-1		
	OC-3		
	OC-12		

Transmit Clock Checks		**Minimum**	**Measured Value**	**Maximum**
Internal Clock Accuracy		51,839,762 Hz		51,840,238 Hz
Transmit Line Frequency Offset	positive	51,844,946 Hz		51,845,422 Hz
	negative	51,834,578 Hz		51,835,054 Hz
BITS Reference Input		0.014891		0.014893

Tributary Checks (Option 22 only)	**Minimum**	**Measured Value**	**Maximum**
DS1 Signal Level	5.0 V		7.0 V

	Passed	**Failed**
DS1 Pulse Shape		
DS1 Bridged Receive Level		
DS1 Monitor Receive Level		
DS1 External Clock Input		

	Minimum	**Measured Value**	**Maximum**
DS3 Signal Level	0.29 V		0.55 V

	Passed	**Failed**
DS3 Pulse Shape		
DS3 Monitor Receive Level		
DS3 External Clock Input		

Table 4–4: CTS 750 (SDH) Test Record

CTS 750 Serial Number:	Temperature and Relative Humidity:
Plug-In Interface Module Type:	Verification Performed by:
Plug-In Interface Module Serial Number:	Date of Verification:

CTS 750 Functional Tests

Test		Passed	Failed
System Self Test with External Loop-Back			
Generated Failures	None		
	LOS		
Pointer Movements	Continuous		

CTS 750 Physical Layer Tests

Transmit Output Checks		Minimum	Measured Value	Maximum
Electrical Signal Level at Transmit Output	STM-1E High Level	900 mV		1.1 V

		Passed	Failed
Electrical Output Pulse Shape	STM-1E		
Optical Output Pulse Shape	STM-1		
	STM-4		
Receive Input Checks		**Passed**	**Failed**
Electrical Input Sensitivity	STM-1E High (part 1)		
	STM-1E High (part 2)		
	STM-1E Cross Connect		
	STM-1E Low		
	STM-1E Monitor		
Optical Input Sensitivity	STM-1		
	STM-4		

Transmit Clock Checks		Minimum	Measured Value	Maximum
Internal Clock Accuracy		51,839,762 Hz		51,840,238 Hz
Transmit Line Frequency Offset	positive	51,844,946 Hz		51,845,422 Hz
	negative	51,834,578 Hz		51,835,054 Hz
2 Mb/s Reference Input		0.019752		0.019754

Tributary Checks (Option 36 only)	Passed	Failed
2 Mb/s Balanced Pulse Mask		
2 Mb/s Balanced Monitor Receive Level		
2 Mb/s Balanced Bridged Receive Level		
2 Mb/s Balanced External Clock Input		
2 Mb/s Balanced Cable Equalization		
	Passed	**Failed**
2 Mb/s Unbalanced Pulse Mask		
2 Mb/s Unbalanced Bridged Receive Level		
2 Mb/s Unbalanced Monitor Receive Level		
2 Mb/s Unbalanced External Clock Input		
	Passed	**Failed**
34 Mb/s Transmit Pulse Mask		
34 Mb/s Monitor Receive Level		
34 Mb/s External Clock Input		
34 Mb/s Cable Equalization		
	Passed	**Failed**
140 Mb/s Pulse Mask		
140 Mb/s Bridged Receive Level		
140 Mb/s Monitor Receive Level		
140 Mb/s External Clock Input		
140 Mb/s Cable Equalization		

Low-Frequency Jitter Tests (Option 14 only)			Jitter Measurement Tests		
Jitter Frequency	**Jitter Amplitude**	**Transmit Rate**	**Minimum**	**Measured Value**	**Maximum**
15 Hz	200 UI Amplitude	2 Mb/s (Unbalanced)	189.25 UI		209.87 UI
		34 Mb/s	189.35 UI		209.77 UI
		140 Mb/s	189.35 UI		209.77 UI
		STM-0E	189.35 UI		209.77 UI
		STM-1E	189.35 UI		209.77 UI
		STM-4	188.80 UI		210.32 UI
150 Hz Jitter Frequency	16 UI Amplitude	2 Mb/s (Unbalanced)	14.95 UI		16.97 UI
		34 Mb/s	15.05 UI		16.87 UI
		140 Mb/s	15.05 UI		16.87 UI
		STM-0E	15.05 UI		16.87 UI
		STM-1E	15.05 UI		16.87 UI
		STM-4	14.90 UI		17.02 UI

High-Amplitude Jitter Tests (Option 14 only)		Jitter Generation Tests			Jitter Measurement Tests		
Transmit/ Clock Rate	**Jitter Frequency**	**Minimum**	**Measured Value**	**Maximum**	**Minimum**	**Measured Value**	**Maximum**
2 Mb/s (Unbalanced)	2.5 kHz	1.64 UI		1.88 UI	1.635 UI		1.885 UI
2 Mb/s (Unbalanced)	1.8 kHz	8.28 UI		9.22 UI	8.17 UI		9.33 UI
2 Mb/s (Unbalanced)	6.4 kHz	2.58 UI		2.92 UI	2.570 UI		2.925 UI
2 Mb/s (Unbalanced)	100 kHz	0.70 UI		0.83 UI	—	*— (not tested)*	—
34 Mb/s	2.5 kHz	1.64 UI		1.88 UI	1.630 UI		1.885 UI
34 Mb/s	8 kHz	8.28 UI		9.22 UI	8.27 UI		9.23 UI
34 Mb/s	26 kHz	2.58 UI		2.92 UI	2.570 UI		2.925 UI
34 Mb/s	100 kHz	0.70 UI		0.83 UI	0.685 UI		0.845 UI
34 Mb/s	800 kHz	0.70 UI		0.83 UI	—	*— (not tested)*	—
140 Mb/s	2.5 kHz	1.63 UI		1.89 UI	1.625 UI		1.880 UI
140 Mb/s	10 kHz	8.27 UI		9.23 UI	8.27 UI		9.23 UI
140 Mb/s	50 kHz	2.57 UI		2.93 UI	2.570 UI		2.925 UI
140 Mb/s	3.5 MHz	0.69 UI		0.84 UI	—	*— (not tested)*	—

Transmit/ Clock Rate	Jitter Frequency	Minimum	Measured Value	Maximum	Minimum	Measured Value	Maximum
STM-0E	2.5 kHz	1.64 UI		1.88 UI	1.630 UI		1.885 UI
STM-0E	5 kHz	1.64 UI		1.88 UI	1.630 UI		1.890 UI
STM-0E	10 kHz	8.28 UI		9.22 UI	8.270 UI		9.230 UI
STM-0E	26 kHz	2.58 UI		2.92 UI	2.570 UI		2.925 UI
STM-0E	400 kHz	0.70 UI		0.83 UI	—	*— (not tested)*	—
STM-1E	5 kHz	1.63 UI		1.89 UI	1.625 UI		1.880 UI
STM-1E	10 kHz	8.28 UI		9.22 UI	8.27 UI		9.23 UI
STM-1E	26 kHz	5.42 UI		6.08 UI	5.420 UI		6.075 UI
STM-1E	1.3 MHz	0.69 UI		0.84 UI	—	*— (not tested)*	—
STM-4	10 kHz *(first test)*	1.56 UI		1.96 UI	1.590 UI		1.915 UI
STM-4	10 kHz *(second test)*	8.20 UI		9.30 UI	8.19 UI		9.22 UI
STM-4	68 kHz	5.35 UI		6.15 UI	5.385 UI		6.110 UI
STM-4	600 kHz	0.62 UI		0.91 UI	0.605 UI		0.810 UI

Low-Amplitude Jitter Tests (Option 14 only)		Jitter Generation Tests			Jitter Measurement Tests		
Transmit Rate	Jitter Frequency	Minimum	Calculated Value = J	Maximum	Minimum	Measured Value	Maximum
2 Mb/s (Unbalanced)	50 kHz	0.266 UI		0.356 UI	J – 0.061 UI		J + 0.049 UI
2 Mb/s (Unbalanced)	100 kHz	0.266 UI		0.356 UI	J – 0.151 UI		J – 0.029 UI
34 Mb/s	800 kHz	0.447 UI		0.557 UI	J – 0.207 UI		J – 0.077 UI
140 Mb/s	400 kHz	0.437 UI		0.567 UI	J – 0.062 UI		J + 0.068 UI
140 Mb/s	3.5 MHz	0.437 UI		0.567 UI	J – 0.207 UI		J – 0.077 UI
STM-0E	400 kHz	0.447 UI		0.557 UI	J – 0.207 UI		J – 0.077 UI
STM-1E	650 kHz	0.437 UI		0.567 UI	J – 0.067 UI		J + 0.063 UI
STM-1E	1.3 MHz	0.437 UI		0.567 UI	J – 0.207 UI		J – 0.077 UI
STM-4	3 MHz	0.186 UI		0.436 UI	J – 0.101 UI		J + 0.079 UI

Self Test

This procedure uses internal routines to verify that the CTS 710 SONET Test Set or the CTS 750 SDH Test Set passes its internal self tests.

Equipment Required	No test equipment or connections are required
Prerequisites	Power up the CTS and allow a twenty minute warm-up period before running self test
Time Required	Approximately five minutes (after warm-up time)

Running Self Test

Set up and execute the self test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys: Internal
		Self Test Control	Run

When the self test completes, the message PASSED appears in the display. If you see the message FAILED, repeat the self test. If the problem persists, contact your local Tektronix field office or representative for assistance.

There are advantages and disadvantages of this self test. One advantage is you do not have to disconnect the CTS from your application. One disadvantage is the electrical and optical I/O circuitry is not verified by the test. If the self test passes and you are still experiencing difficulty, perform *System Self Test with External Loop-Back* on page 4–16 to test the electrical I/O circuitry.

Functional Tests

The purpose of functional tests is to verify the functional specifications of the CTS. Most functional tests rely on the front panel status lights to indicate the results of the test. Figure 4–2 shows the status lights for a CTS 710 with Option 22.

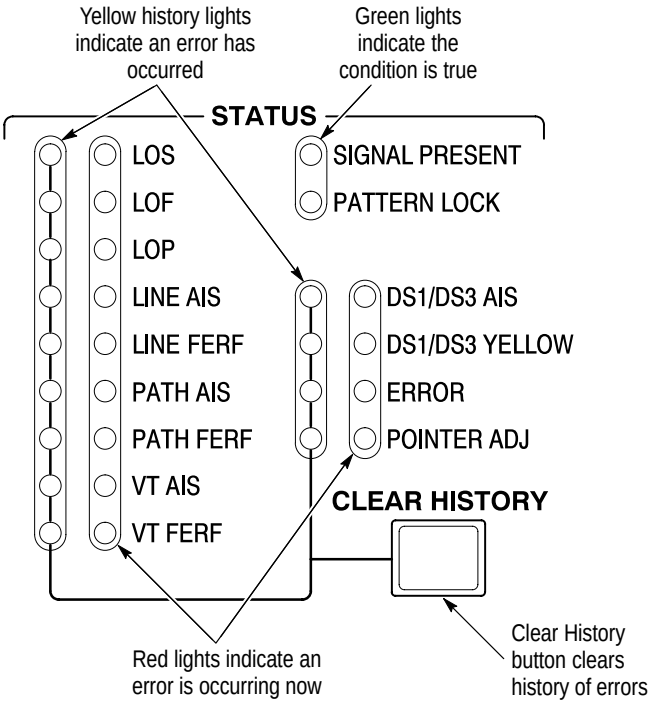


Figure 4–2: Typical Front-Panel Status Lights

Loop-Back Connection

Each functional test requires an external loop-back connection from the TRANSMIT output to the RECEIVE input. For the electrical loop-back, you can use the 75 Ω BNC coaxial cable provided as a standard accessory to the CTS. If one of the Electrical/Optical Plug-In Interface Modules is installed in your CTS, you also need a short optical cable that is compatible with the optical connectors on your instrument. If your CTS has Option 05, connect a 10 dB optical attenuator (included with Option 05) in series with the cable to prevent saturation of the receiver input. Optical cables are not included as standard accessories to the CTS.

How to Proceed

If the CTS fails any of these tests, it has failed the performance verification. Double check the electrical and optical connections and repeat any failed test. If the failure persists, contact your local Tektronix field office or representative for assistance.

You may perform the functional tests in any order. Each test is independent and does not depend on the setup from the previous test.

System Self Test with External Loop-Back

This test runs the self test including coverage of the transmitter and receiver I/O circuitry and, if installed, Option 22 or Option 36.

Equipment Required	75 Ω BNC coaxial cable (item 19) for electrical loop-back, one required (two required if Option 22 or Option 36 is installed) Optical loop-back cable (item 13) if Electrical/Optical Plug-In Interface Module is installed 10 dB optical attenuator (item 14) if Option 05 is installed. If Option 22 is installed, 100 Ω Bantam-to-Bantam Cable (item 29) for electrical loop-back If Option 36 is installed, 120 Ω DIN41628L cable (item 34) for electrical loop-back
Prerequisites	CTS warmed-up at least twenty minutes
Time Required	Approximately five minutes

1. Attach electrical and optical loop-back cables from the TRANSMIT outputs to the RECEIVE inputs (include optical attenuator if Option 05).
2. If Option 22 or Option 36 is installed, attach the electrical loop-back cables from the TRANSMIT/DROP outputs to the RECEIVE/ADD inputs.
3. Set up and execute the system self test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys Ext
		Self Test Control	Run

4. Read the diagnostic result on the display when the test has completed.

Generated Failures

This test checks that the CTS detects the LOS failure correctly.

Equipment Required	75 Ω BNC coaxial cable (item 19) for electrical loop-back
Prerequisites	CTS warmed-up at least twenty minutes
Time Required	Approximately two minutes

1. Attach the 75 Ω coaxial cable (electrical) from the TRANSMIT output to the RECEIVE input.
2. Perform the initial setup of the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3 or STM-1E
		Tx/Rx Settings	Coupled

3. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.
4. Press the **CLEAR HISTORY** button, wait two seconds, and then verify that no yellow history lights are on.
5. Remove one end of the 75 Ω coaxial cable from the Transmit Output to the Receive Input.
6. Verify that the LOS light is on.
7. Replace the 75 Ω coaxial cable from the Transmit Output to the Receive Input.
8. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.
9. Press the **CLEAR HISTORY** button, wait two seconds, and then verify that no yellow history lights are on.

Pointer Movement

This test checks that the CTS generates and measures pointer movement correctly.

Equipment Required	75 Ω BNC coaxial cable (item 19) for electrical loop-back
Prerequisites	CTS warmed-up at least twenty minutes
Time Required	Approximately four minutes

1. Attach the 75 Ω coaxial cable (electrical) from the TRANSMIT output to the RECEIVE input.
2. To verify Continuous Pointer Movements, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3 or STM-1E
		Tx/Rx Settings	Coupled
TRANSMIT	POINTERS & TIMING	Pointer Control	Continuous
		Pointer Rate	Max 2 ms
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED

3. Press the **Minutes** button and then rotate the knob to **1 m**.
4. Press the **Seconds** button and then rotate the knob to **40 s**.
5. Press the **Done** button to set the test duration to 1 minute, 40 seconds (100 seconds, total).
6. To monitor pointer movements, change the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
RESULTS	MAIN RESULTS	*none*	Pointers

7. Press the **START/STOP** button, and verify that the START/STOP light is on.

8. Wait 100 seconds for the test to complete. When the START/STOP light turns off, verify that the Positive Justification and Negative Justification counts meet both of the following conditions:

$$24000 \leq \textit{Positive Justifications} \leq 26000$$

$$\textit{Negative Justifications} = \textit{Positive Justifications} \pm 1$$

9. Verify that the yellow **ERROR** history light is off.

Physical Layer Tests

This section contains a set of procedures that verify the CTS 710 SONET Test Set or the CTS 750 SDH Test Set meets its physical layer specifications. These procedures check performance of the standard instrument as well as two optional Plug-In Interface Modules, so some steps may not apply to your CTS. The steps that apply only to optional Plug-In Interface Modules are identified in the procedures.

The procedures contain setup instructions for the example equipment listed in Table 4–2, *Required Test Equipment*, which begins on page 4–4. You may use equipment other than the recommended examples if it meets the minimum requirements listed. However, if you do, you might need to modify the interconnect diagrams and setup instructions.

Prerequisites for All Physical Layer Tests

The procedures in this section are a valid test of the CTS performance when the following requirements are met:

- The cabinet must be installed on the CTS.
- The CTS has passed all the *Functional Tests*, which begin on page 4–15.
- The CTS has warmed up for at least 20 minutes and is operating in an ambient temperature between 0° C and +50° C.

Sequence of Tests

Most tests are dependent on those that precede them, so perform all the procedures in sequential order.

Check Electrical Output Signal Level at Transmit Output (High Level)

This test checks the high-level signal amplitude directly at the TRANSMIT output connector. The amplitude value measured in this test accounts for the difference between the 75 Ω source impedance of the TRANSMIT output and the 50 Ω input impedance of the communications signal analyzer.

Equipment Required	Communications signal analyzer (item 4) 75 Ω coaxial cable (item 19) SMA male to BNC female adapter (item 23) BMP-5075R 75 Ω female BNC to 50 Ω male BNC (item 43)
Prerequisites	All prerequisites listed on page 4–20 All previous tests
Time Required	Approximately ten minutes

1. Connect the CTS TRANSMIT output to the communications signal analyzer input as shown in Figure 4–3.

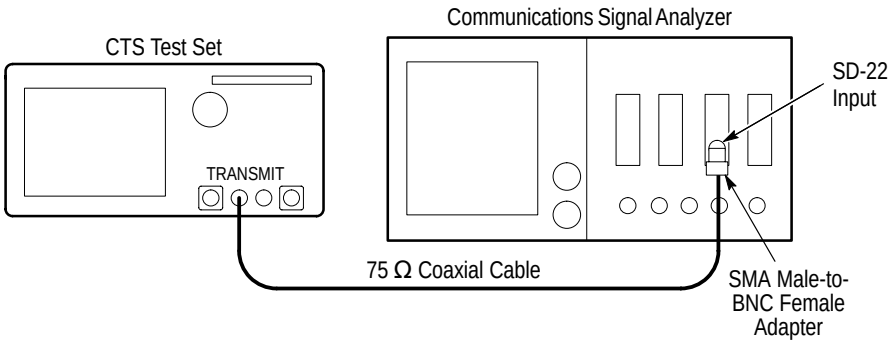


Figure 4–3: Transmit Electrical Output Amplitude Hookup

2. To characterize the 75 Ω to 50 Ω conversion, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3 or STM-1E
		Transmit Level	High or 0 dB

3. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select **Initialize** in the pop-up menu.

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   c. Select the **TRIGGER** menu. Set the Source to **Internal Clock**.

   d. Select the **DISPLAY MODES** menu.

   e. Select the **Persist/Histograms** pop-up menu, select the **Normal** menu item, and then select **Exit**.

f. Select the **WAVEFORM** menu, select the **Horizontal Desc** pop-up menu, and set Main Record Length to **5120 pts**.

g. Set the Vertical Size to **100 mV/div**.

h. Set the Horizontal Size to **1 µs/div**.

NOTE. *For increased accuracy, you may perform a LOOP Gain adjustment of the SD22 head on the communications signal analyzer. If you need instructions, refer to the communications signal analyzer and SD22 user manuals.*

i. Select the **MEASURE** menu and then the **Measurements** pop-up menu.

j. Select the **Pk-Pk** measurement, and then select **Exit**.

k. Select **Pk-Pk** on the menu screen, and measure the Mean value of the amplitude measurement after 32 acquisitions have completed. Record this value as **V1**.

l. Connect the CTS TRANSMIT output to the communications signal analyzer as shown in Figure 4–4.

m. Set the Vertical Size to **100 mV/div**.

n. Select the **MEASURE** menu and then the **Measurements** pop-up menu.

o. Select the **Pk-Pk** measurement, and then select **Exit**.

p. Select **Pk-Pk** on the menu screen, and measure the Mean value of the amplitude measurement after 32 acquisitions have completed. Record this value as **V2**.

NOTE. *The following waveform description accounts for the loss of the impedance converter, splitter, and 50Ω measurement impedance. This waveform description should be used for all of the following amplitude measurements.*

q. Select the **WAVEFORM** menu, select the **Vertical Desc** pop-up menu, and enter the description **M1*((<V1 voltage>/<V2 voltage>)/0.80)**.

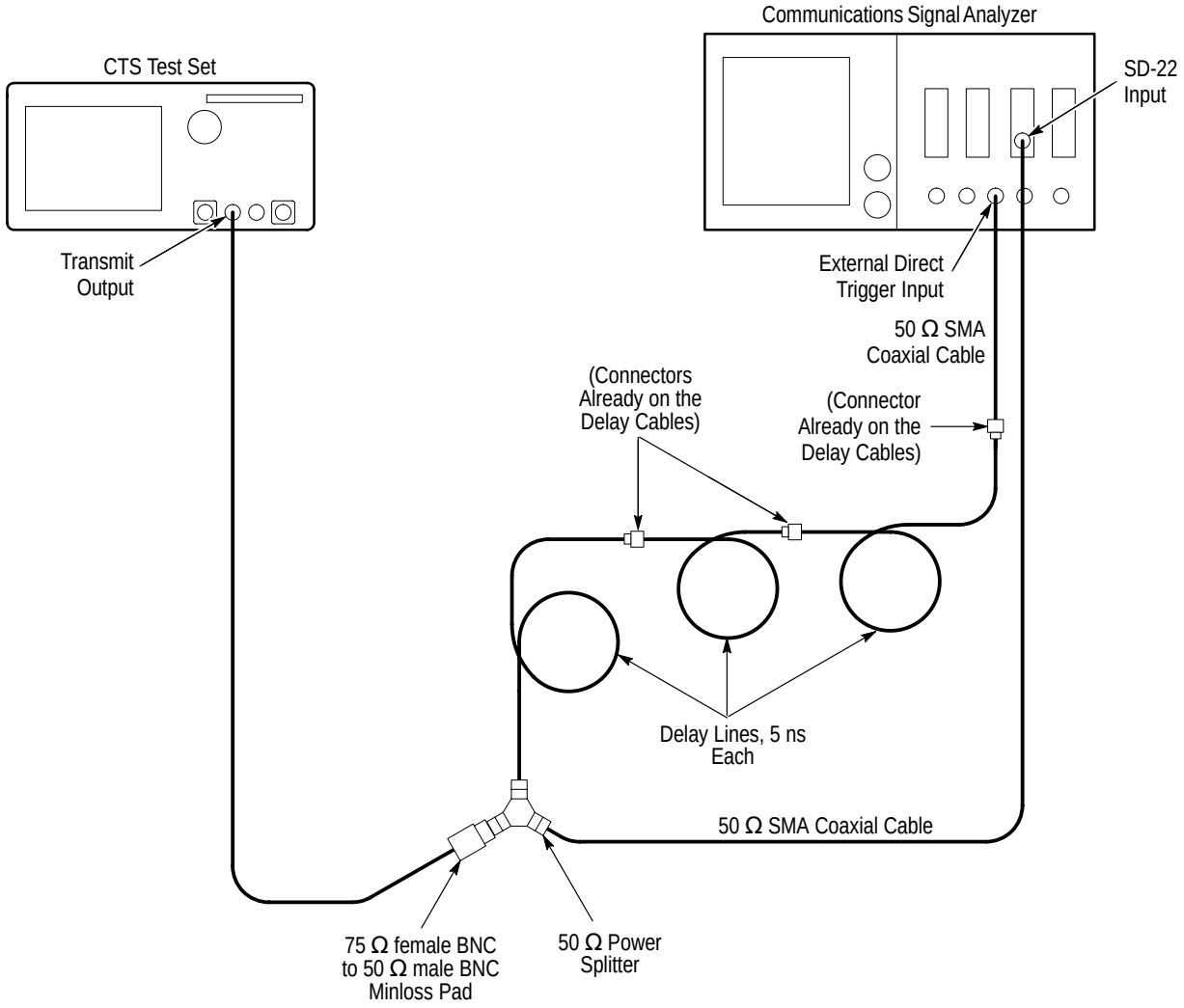


Figure 4–4: Transmit Level Hookup

4. If you are verifying a CTS 750, skip to step 6. To set up the CTS to output a STS-1 cross connect level, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-1
		Transmit Level	Cross Connect

5. Set up the communications signal analyzer with the following steps:

a. Select the **WAVEFORM** menu, and set the Vertical Size to **200 mV/div**.

b. Set the Horizontal Main Size to **10 ns/div**.

c. Select the **Vertical Desc** pop-up menu, and enter the description **M1*((<V1 voltage>/<V2 voltage>)/0.80)**.

d. Set the Horizontal Desc to **512 points**.

e. Select the **Persist/Histograms** pop-up menu, select the **Variable** menu item, and then select **Exit**.

f. Select the **TRIGGER** menu. Set the **Source** to **External Direct**, and adjust the Level for a stable display.

g. Select the **Cursors Icon**, and set the Cursor Type to **Horizontal Bars**.

h. Move the cursors to the approximate center of the peaks of the waveform, and measure the cursor voltage.

i. Verify that the voltage is between 0.90 V and 1.10 $V_{pk\text{-}pk}$.

6. To set up the CTS to output a STS-3 or STM-1 high level, do the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3 or STM-1E
		Transmit Level	High or 0 dB

7. Set up the communications signal analyzer with the following steps:

a. Select the **WAVEFORM** menu, and set the Vertical Size to **200 mV/div**.

b. Set the Horizontal Main Size to **2 ns/div**.

c. Select the **Vertical Desc** pop-up menu, and enter the description **M1*((<V1 voltage>/<V2 voltage>)/0.80)**.

d. Select the **TRIGGER** menu. Set the **Source** to **External Direct**, and adjust the Level for a stable display.

e. Select the **DISPLAY MODES** menu.

f. Select the **Persist/Histograms** pop-up menu, select the **Variable** menu item, and then select **Exit**.

g. Select the **MEASURE** menu and then the **Measurements** pop-up menu.

h. Select the **Amplitude** measurement, and then select **Exit**.

i. Select **Amplitude** on the menu screen, and measure the Mean value of the amplitude measurement.

j. Verify that the voltage is between 0.900 V and 1.100 $V_{pk\text{-}pk}$.

Check Electrical Output Pulse Shape at Transmit Output (High Level) and at Cross Connect

This test checks the high- and cross-connect-level signal pulse shapes. The signals are equalized through appropriate lengths of reference cable for comparison with eye masks specified in ANSI T1.102, Bellcore TR-NWT-000253, and ITU G.703.

Equipment Required	Communications signal analyzer (item 4) 225 ft (68.6 m) length of 75 Ω reference cable (item 16), two required 75 Ω to 50 Ω Impedance Converter (item 18) 75 Ω coaxial cable (item 19) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) Delay line (item 24) BNC female-to-BNC female adapter (item 26)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately twenty minutes

1. Perform an automatic gain calibration on the communications analyzer and an auto offset calibration with the following steps:

   a. Connect a coaxial cable from the **CALIBRATE OUTPUT** to the channel to be used.

   b. Select the **WAVEFORM** menu.

   c. Select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

   d. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   e. Select the **UTILITY** menu, and then select the **Page to Enhanced Accuracy** pop-up menu.

   f. Select the **Gain** menu, **Automatic Calibrate**, and then **Proceed**.

   g. Select **Store Constants**, and then **Exit**.

h. Disconnect the coaxial cable.

i. Connect a 50 Ω terminator to the channel to be used.

j. Select the **Offset** menu, **Automatic Calibrate**, and then **Proceed**.

k. Select **Store Constants**, and then **Exit**.

2. Connect the CTS TRANSMIT output to the communications signal analyzer as shown in Figure 4–5.

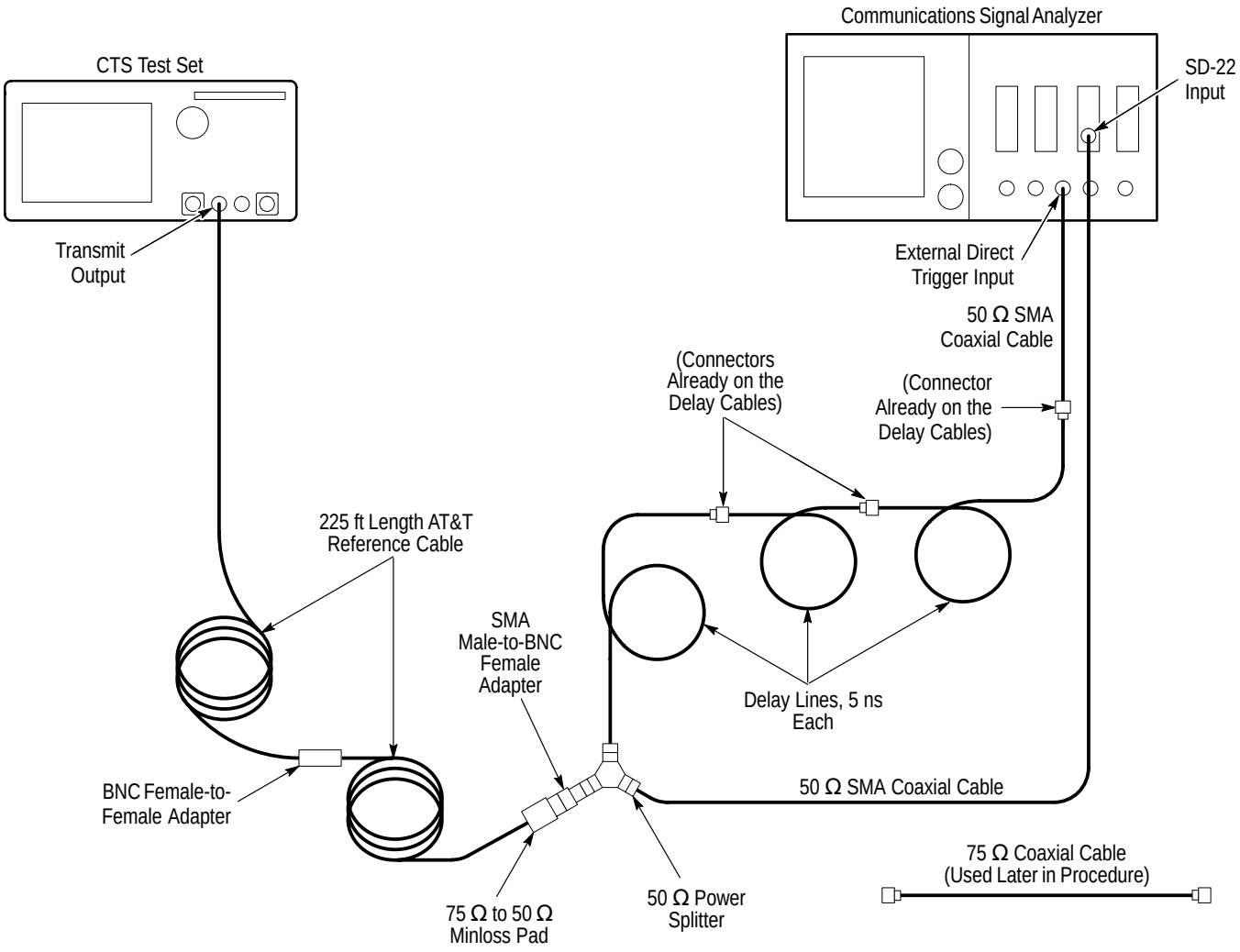


Figure 4–5: Transmit Electrical Output Pulse Shape Hookup

3. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and the **Initialize** menu item in the pop-up menu.

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   c. Select the **TRIGGER** menu, set the **Slope** to **–**.

   d. Select the **DISPLAY MODES** menu.

   e. Select the **Persist/Histograms** pop-up menu, select the **Color Grading** menu item, and then select **Exit**.

   f. Select the **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

   g. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs) then enter the numeric value **100** followed by **Enter**.

   h. If you are verifying the CTS 750, skip to step 17 on page 4–31. To verify the STS-1 pulse shape (CTS 710 only), select the **Standard Masks** pop-up menu and then the **STS-1 51.840 Mb** menu item from the set of built-in ANSI T1.102 Electrical Standards masks.

4. To generate the STS-1 signal, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-1
		Transmit Level	High

5. Perform the test with the following sequence on the communications signal analyzer:

   a. Select the **DISPLAY MODES** menu.

   b. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

   c. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

   d. Select the **Stop N Waveforms** menu item.

e. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

6. Remove both 225 ft (68.6 m) lengths of 75 Ω reference cable and the BNC female-to-BNC female adapter. Reconnect the CTS to the minloss pad with the short (≈1 m) 75 Ω coaxial cable that has not been used until this step in the procedure.

7. To verify the STSX-1 pulse shape, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-1
		Transmit Level	Cross Connect

8. Perform the test with the following sequence on the communications signal analyzer:

a. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

b. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

c. Select the **Stop N Waveforms** menu item.

d. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

9. To verify the STS-3 pulse shape, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3
		Transmit Level	High

10. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Select the **TRIGGER** menu, set the **Slope** to **+**, and then select **Exit**.

b. Select the **DISPLAY MODES** menu.

c. Select the **Standard Masks** pop-up menu and then the **STS-3 155.52 Mb** menu item from the set of built-in ANSI T1.102 Electrical Standards masks.

d. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

NOTE. *In some instances, AutoSet may not adjust the waveform amplitude, offset, and/or horizontal positioning to the optimum settings for a particular mask test. If the test fails, slightly readjust the vertical scale and offset, and also the horizontal position to improve waveform alignment.*

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e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

g. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

11. To verify the STSX-3 pulse shape, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	Cross Connect

12. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Select the **Standard Masks** pop-up menu and then the **STSX-3 155.52 Mb** menu item from the set of built-in ANSI T1.102 Electrical Standards masks.

b. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

c. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

d. Select the **Stop N Waveforms** menu item.

e. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

13. Remove the short (≈ 1 m) length of 75 Ω coaxial cable and replace it with one 225 ft (68.6 m) length of 75 Ω reference cable.

14. To verify the STS-3 pulse shape at cross connect, set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High

15. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

b. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

c. Select the **Stop N Waveforms** menu item.

NOTE. *In some instances, AutoSet may not adjust the waveform amplitude, offset, and/or horizontal positioning to the optimum settings for a particular mask test. If the test fails, slightly readjust the vertical scale and offset, and also the horizontal position to improve waveform alignment.*

d. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

16. If you are verifying a CTS 710, you are finished with this test; continue with the next test, *Check Optical Output Pulse Shape*, on page 4–33. If you are verifying a CTS 750, proceed with the following steps.

17. Remove both 225 ft (68.6 m) lengths of 75 Ω reference cable and replace them with the short (≈1 m) 75 Ω coaxial cable.

18. To verify the STM-1E pulse shape, set up the CTS 750 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM-1E
		Transmit Level	High or 0 dB

19. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Select the **TRIGGER** menu, set the **Slope** to +.

b. Select the **DISPLAY MODES** menu.

c. Select the **Standard Masks** pop-up menu and then the **STM1 155.52 Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

d. Press the **AUTOSET** button on the front panel of the communications signal analyzer. You may have to reposition the signal vertically.

e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

NOTE. *In some instances, AutoSet may not adjust the waveform amplitude, offset, and/or horizontal positioning to the optimum settings for a particular mask test. If the test fails, slightly readjust the vertical scale and offset, and also the horizontal position to improve waveform alignment.*

g. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check Optical Output Pulse Shape

These tests verify the signal shape of the transmitted optical output pulse by comparing with eye masks as specified in Bellcore TR-NWT-000253 and ITU G.703. These tests apply only if your CTS has one of the optional Electrical/Optical Plug-In Interface Modules installed. If your CTS does not have optical capability, proceed to *Check Electrical Input Sensitivity,* which begins on page 4–37.

Equipment Required	Communications signal analyzer (item 4) Optical attenuator (item 6) SDH/SONET Reference Receiver and Power Meter (item 7, 9, 10, or 11, depending on CTS configuration) Optical fiber cable (item 13) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22) SMA male-to-BNC female adapter (item 23) Delay line (item 24) 50 Ω BNC coaxial cable (item 25)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately twenty minutes

1. Connect the CTS, optical attenuator, reference receiver, optical power meter, and communications signal analyzer as shown in Figure 4–6.
2. Set the optical attenuator attenuation to **0 dB**.
3. If your CTS has Option 03 or Option 04, set the optical attenuator and optical power meter wavelengths to **1310 nm**. If your CTS has Option 05, set the optical attenuator and optical power meter wavelengths to **1550 nm**.
4. Set the optical power meter measurements to **dBm**.

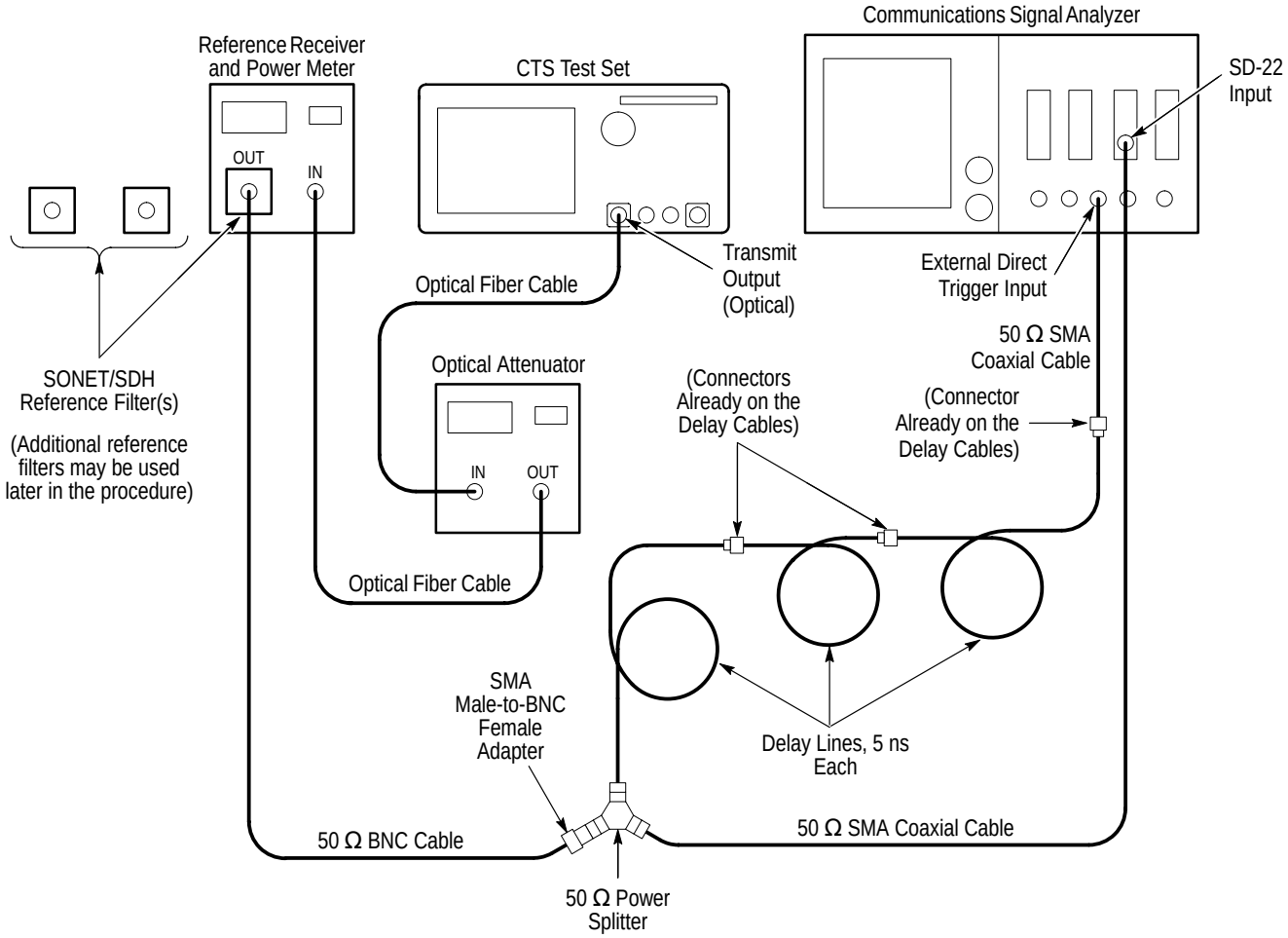

Figure 4–6: Transmit Optical Output Pulse Shape Hookup

5. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu**.**

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   c. Select the **TRIGGER** menu, set the **Slope** to +.

   d. Select the **DISPLAY MODES** menu.

   e. Select the **Persist/Histograms** pop-up menu, select the **Color Grading** menu item, and then select **Exit**.

f. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

g. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs), and then enter the numeric value **100** followed by **Enter**.

h. If you are verifying the CTS 750, skip to step 10. To verify the CTS 710 OC-1 pulse shape, select the **Standard Masks** pop-up menu and then the **OC-1 51.84 Mb** menu item from the set of built-in ANSI SONET Optical Standards masks.

6. Install the FS52 Filter at the OUTPUT of the SONET Reference Receiver and Power Meter, and then connect the 50 Ω coaxial cable to the FS52 Filter.

7. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-1

8. If your CTS has Option 03 or Option 04, verify that the measurement on the optical power meter is in the range from –7 dBm to –12 dBm. If your CTS has Option 05, set the optical attenuator attenuation so that the optical power meter reading is approximately **–8 dBm**.

9. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

b. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

c. Select the **Stop N Waveforms** menu item.

d. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green **Passing** message displayed in the **Mask Testing** pop-up menu selector.

10. To check the OC-3 or STM-1 optical signal shape, install the FS156 Filter at the OUTPUT of the SDH/SONET Reference Receiver and Power Meter (in place of the FS52 filter, if already installed) and then connect the 50 Ω coaxial cable to the FS156 Filter.

11. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-3 or STM-1

12. If your CTS has Option 03 or Option 04, verify that the measurement on the optical power meter is in the range from –7 dBm to –12 dBm. If your CTS has Option 05, set the optical attenuator attenuation so that the optical power meter reading is approximately **–8 dBm**.

13. Set up and perform the test with the following sequence on the communications signal analyzer:

a. Select the **Standard Masks** pop-up menu and then the **OC-3/STM-1 155.52 Mb** menu item from the set of built-in ANSI SONET Optical Standards masks.

b. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

c. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

d. Select the **Stop N Waveforms** menu item.

e. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

14. If your CTS does not have OC-12 or STM-4 capability (option 04), proceed to *Check Electrical Input Sensitivity*, which begins on page 4–37. To check the OC-12 or STM-4 optical signal shape, install the FS622 Filter in place of the FS156 filter previously installed, and then connect the 50 Ω coaxial cable to the FS622 Filter.

15. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-12 or STM-4

16. Verify that the measurement on the optical power meter is in the range from –7 dBm to –12 dBm.

17. Set up and perform the test with the following sequence on the communications signal analyzer:

    a. Select the **Standard Masks** pop-up menu and then the **OC-12/STM-4 622.08 Mb** menu item from the set of built-in ANSI SONET Optical Standards masks.

    b. Press the **AUTOSET** button on the front panel of the communications signal analyzer.

    c. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

    d. Select the **Stop N Waveforms** menu item.

    e. After 100 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check Electrical Input Sensitivity

This test verifies the receiver electrical sensitivity by receiving an error-free signal at all specified levels.

Equipment Required	100 ft (31 m) length of 75 Ω reference cable (item 15) 225 ft (68.6 m) length of 75 Ω reference cable (item 16), two required 75 Ω Coaxial Cable (item 19) BNC female-to-BNC female adapter (item 26), two required 10X (20 dB) Attenuator (item 38) 2X (6 dB) Attenuator (item 39)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the CTS TRANSMIT output through the 75 Ω coaxial cable to the RECEIVE input as shown in Figure 4–7. You will need the additional items shown later in the procedure.

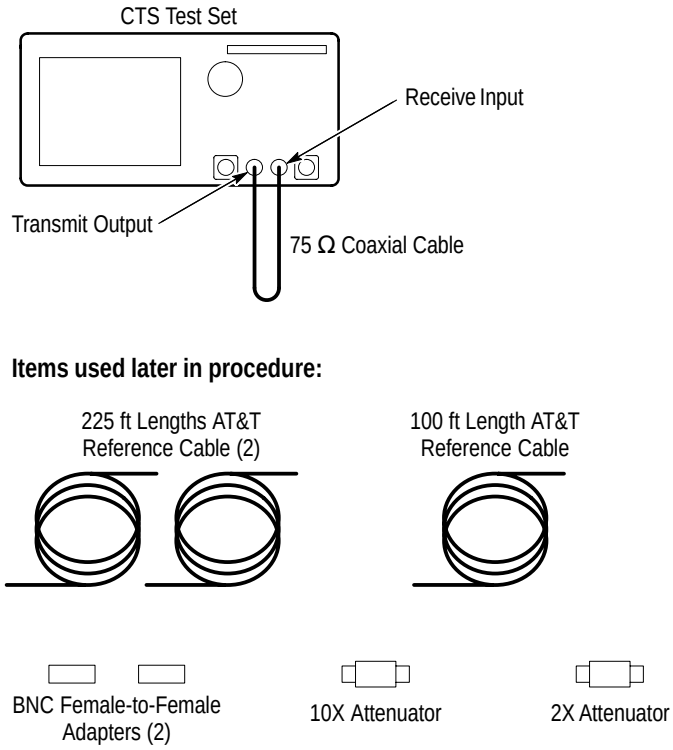

Figure 4–7: Receive Electrical Input Sensitivity Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute

3. Rotate the knob to set the Test Duration to **2 m**, and then press **Done**.

4. If you are verifying a CTS 750, skip to step 22. To verify the STS-1 high-level sensitivity, continue the CTS 710 setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-1
		Transmit Level	High
RECEIVE	RECEIVE SETTINGS	Receive Rate	STS-1
		Receive Level	High
RESULTS	MAIN RESULTS	*none*	Errors

5. Press the **START/STOP** button, and verify that the START/STOP light is on.

6. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

7. Install the 2X attenuator in series with the coaxial cable between the TRANSMIT output and the RECEIVE input.

8. Press the **START/STOP** button, and verify that the START/STOP light is on.

9. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

10. To verify the STS–1 cross connect sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High
RECEIVE	RECEIVE SETTINGS	Receive Level	Cross Connect
RESULTS	MAIN RESULTS	*none*	Errors

11. Install the 2X attenuator, two 225 ft (68.6 m) lengths of reference cable, and one 100 ft (31 m) length of reference cable (550 ft or 168 m, total) between the TRANSMIT output and the RECEIVE input.

12. Press the **START/STOP** button and verify that the START/STOP light is on.

13. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

14. To verify the STS–1 low-level sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	Cross Connect
RECEIVE	RECEIVE SETTINGS	Receive Level	Low
RESULTS	MAIN RESULTS	*none*	Errors

15. Press the **START/STOP** button and verify that the START/STOP light is on.

16. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

17. To verify the STS–1 monitor-level sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

18. Install a 10X attenuator in series with the 2X attenuator, two 225 ft (68.6 m) lengths of reference cable, and one 100 ft (31 m) length of reference cable between the TRANSMIT output and the RECEIVE input (20X attenuation, total).

19. Press the **START/STOP** button and verify that the START/STOP light is on.

20. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

21. Remove the two attenuators and three lengths of reference cable. Install the short (≈1 m) length of 75 Ω coaxial cable between the TRANSMIT output and the RECEIVE input.

22. To verify the STS-3 or STM-1E high-level sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STS-3 or STM-1E
		Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Rate	STS-3 or STM-1E
		Receive Level	High or 0 dB
RESULTS	MAIN RESULTS	*none*	Errors

23. Press the **START/STOP** button and verify that the START/STOP light is on.

24. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

25. Install the 2X attenuator in series with the coaxial cable between the TRANSMIT output and the RECEIVE input.

26. Press the **START/STOP** button, and verify that the START/STOP light is on.

27. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

28. To verify the STS–3 or STM-1E cross connect sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	Cross Connect or –6 dB
RESULTS	MAIN RESULTS	*none*	Errors

29. Install one 225 ft (68.6 m) length of reference cable and one 100 ft (31 m) length of reference cable (325 ft or 100 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

30. Press the **START/STOP** button and verify that the START/STOP light is on.

31. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

32. To verify the STS-3 or STM-1E low-level sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	Low or –12 dB
RESULTS	MAIN RESULTS	*none*	Errors

33. Install two 225 ft (68.6 m) lengths of reference cable and one 100 ft (31 m) length of reference cable (550 ft or 168 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

34. Press the **START/STOP** button and verify that the START/STOP light is on.

35. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

36. To verify the STS–1 monitor-level sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

37. Remove the three reference cables. Install a 10X attenuator and a 2X attenuator (20X total attenuation) in series with the short (≈1 m) length of 75 Ω coaxial cable between the TRANSMIT output and the RECEIVE input.

38. Press the **START/STOP** button and verify that the START/STOP light is on.

39. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

Check Optical Input Sensitivity

These tests verify the sensitivity of the optical receiver. These tests apply only if your CTS has one of the optional Electrical/Optical Plug-In Interface Modules installed. If your CTS does not have optical capability, proceed to *Check Internal Clock Accuracy*, which begins on page 4–46.

Equipment Required	Optical attenuator (item 6) SDH/SONET Reference Receiver and Power Meter (item 7, 9, 10, or 11, depending on CTS configuration) Optical fiber cable (item 13), two required
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately thirty minutes

1. Connect the CTS TRANSMIT output through the optical attenuator to the SDH/SONET Reference Receiver and Power Meter as shown in Figure 4–8.

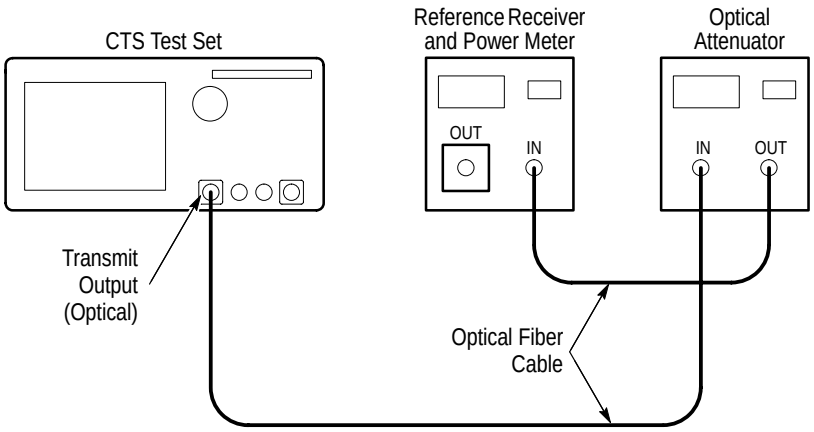

Figure 4–8: Receive Optical Input Sensitivity Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute

3. Rotate the knob to set the Test Duration to **2 m**, and then press **Done**.

4. Set the optical power meter measurement units to **dBm**.

5. If your CTS has Option 03 or Option 04, set the optical attenuator and optical power meter wavelengths to **1310 nm**. If your CTS has Option 05, set the optical attenuator and optical power meter wavelengths to **1550 nm**.

6. If you are verifying a CTS 750, skip to step 11. To verify the OC-1 sensitivity, continue the CTS 710 setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-1
		Tx/Rx Settings	Coupled
RESULTS	MAIN RESULTS	*none*	Errors

7. Set the optical attenuator attenuation so that the optical power meter reading is **–28 dBm**.

8. Remove the fiber connection from the optical power meter and connect it to the RECEIVE input of the CTS.

9. Perform the test with the following steps:

   a. Press the **START/STOP** button, and verify that the START/STOP light is on.

   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

   c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

10. Remove the fiber connection from the RECEIVE input of the CTS, and connect it to the optical power meter.

11. To verify the OC-3 or STM-1 sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-3 or STM-1
		Tx/Rx Settings	Coupled
RESULTS	MAIN RESULTS	*none*	Errors

12. Set the optical attenuator attenuation so that the optical power meter reading is **–28 dBm**.

13. Remove the fiber connection from the optical power meter, and connect it to the RECEIVE input of the CTS.

14. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

15. Remove the fiber connection from the RECEIVE input of the CTS, and connect it to the optical power meter.

16. If your CTS does not have OC-12 or STM-4 capability (option 04), proceed to *Check Internal Clock Accuracy*, which begins on page 4–46. To verify the OC-12 or STM-4 sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	OC-12 or STM-4
RESULTS	MAIN RESULTS	*none*	Errors

17. Set the optical attenuator attenuation so that the optical power meter reading is **–28 dBm**.

18. Remove the fiber connection from the optical power meter, and connect it to the RECEIVE input of the CTS.

19. Perform the test with the following steps:

a. Press the **START/STOP** button, and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

Check Internal Clock Accuracy

This test verifies the accuracy of the internal clock at its base frequency of 51.84 MHz. All internally generated transmit clock rates are derived from exact harmonics (1x, 3x, or 12x) of this base frequency. Therefore, the accuracies of all transmit line rates are indirectly verified by this test.

Equipment Required	Universal Counter/Timer (item 1) 50 Ω SMB-to-BNC coaxial cable (item 28)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CAL output (CTS rear panel) to the Universal Counter/Timer input as shown in Figure 4–9.

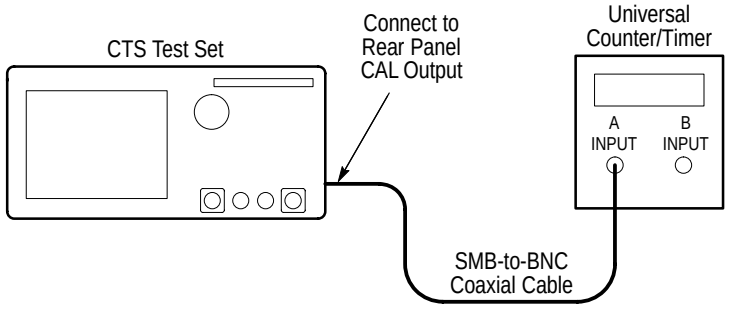

Figure 4–9: Internal Clock Accuracy Hookup

2. To verify the internal clock accuracy, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup

3. Make the following settings on the Universal Counter/Timer:
   a. Set input impedance to **50 Ω**.
   b. Set input coupling to **AC**.
   c. If you are using a Tektronix DC5010 counter, set the averages to $\mathbf{10^8}$. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the HP53131A/132A Universal Counter operating guide, part number 53131-90021, pages 1-5, 2-7, 2-8, and 2-16, for instructions on how to set **DIGITS**).
   d. Set measurement mode to **Frequency**.
4. Verify that the Universal Counter/Timer reads between 51,839,762 Hz and 51,840,238 Hz (inclusive).

Check Transmit Line Frequency Offset

This test verifies the transmit line frequency offset for all instruments except the CTS 750 with Option 14. If you are verifying a CTS 750 with Option 14, proceed to the next check.

This test verifies the transmit line frequency offset at the base clock frequency of 51.84 MHz. All internally generated transmit clock rates are derived from exact harmonics (1x, 3x, or 12x) of this base frequency. Therefore, the frequency offset of all transmit line rates is indirectly verified by this test.

Equipment Required	Universal Counter/Timer (item 1) 50 Ω SMB-to-BNC coaxial cable (item 28)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CAL output (CTS rear panel) to the Universal Counter/Timer input as shown in Figure 4–10 (same setup as previous test).

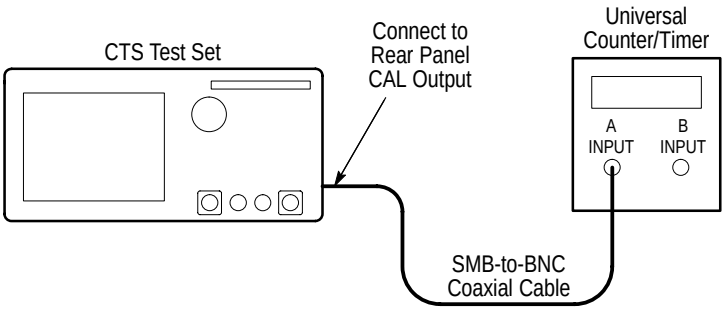

Figure 4–10: Transmit Line Frequency Offset Hookup

2. To verify the transmit line frequency offset, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	POINTERS & TIMING	Pointer/Timing Mode	Frequency Offset
		Frequency Offset	MAX +100 ppm

3. Make the following settings on the Universal Counter/Timer:

   a. Set input impedance to **50 Ω**.

   b. Set input coupling to **AC**.

   c. If you are using a Tektronix DC5010 counter, set the averages to $\mathbf{10^8}$. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the HP53131A/132A Universal Counter operating guide, part number 53131-90021, pages 1-5, 2-7, 2-8, and 2-16, for instructions on how to set **DIGITS**).

   d. Set measurement mode to **Frequency**.

4. Verify that the Universal Counter/Timer reads between 51,844,946 Hz and 51,845,422 Hz (inclusive).

5. To test negative transmit line frequency offset, change the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	POINTERS & TIMING	Frequency Offset	USER DEFINED
		Frequency Offset	Coarse

6. Rotate the knob to set the Frequency Offset to **–100 ppm**, and then press **Done**.

7. Verify that the Universal Counter/Timer reads between 51,834,578 Hz and 51,835,054 Hz (inclusive).

Check Transmit Line Frequency Offset (CTS 750 Option 14 only)

This test verifies the transmit line frequency offset for the CTS 750 with Option 14. Use the previous test for all other instrument configurations.

This test verifies the transmit line frequency offset at the base clock frequency of 51.84 MHz. All internally generated transmit clock rates are derived from exact harmonics (1x, 3x, or 12x) of this base frequency. Therefore, the frequency offset of all transmit line rates is indirectly verified by this test.

Equipment Required	Universal Counter/Timer (item 1) 75 Ω BNC coaxial cable (item 19) 75 Ω to 50 Ω impedance converter (item 18)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the J/CLK output (CTS rear panel) to the Universal Counter/Timer input as shown in Figure 4–11.

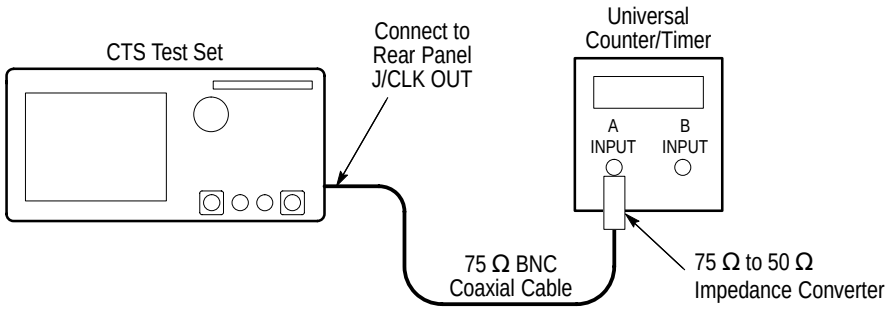

Figure 4–11: Transmit Line Frequency Offset Hookup

2. To verify the transmit line frequency offset, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	Off
		Jitter Output	Clock 0.8 V
		Jitter Clock Rate	52 MHz (STM-0)
		Jitter Clock Offset	+100 ppm

3. Make the following settings on the Universal Counter/Timer:

   a. Set input impedance to **50 Ω**.

   b. Set input coupling to **AC**.

   c. If you are using a Tektronix DC5010 counter, set the averages to $\mathbf{10^8}$. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the HP53131A/132A Universal Counter operating guide, part number 53131-90021, pages 1-5, 2-7, 2-8, and 2-16, for instructions on how to set **DIGITS**).

   d. Set measurement mode to **Frequency**.

4. Verify that the Universal Counter/Timer reads between 51,844,946 Hz and 51,845,422 Hz (inclusive).

5. To test negative transmit line frequency offset, change the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Clock Offset	USER DEFINED
		Frequency Offset	Coarse

6. Rotate the knob to set the Frequency Offset to **–100 ppm**, and then press **Done**.

7. Verify that the Universal Counter/Timer reads between 51,834,578 Hz and 51,835,054 Hz (inclusive).

Check Frequency Lock to BITS Reference (CTS 710 only)

This test only applies to the CTS 710. If you are testing a CTS 750, proceed to the next test, *Check Frequency Lock to 2 Mb/s Reference*, on page 4–53.

This test verifies that the transmit clock in the CTS 710 is able to lock to the 1.544 Mb/s BITS Reference Input. This test measures the frequency ratio of a synthesized BITS Reference signal to the transmit clock in order to verify the frequency-locked condition. The transmit clock frequency is measured at the CAL output on the rear panel of the CTS 710.

Equipment Required	Universal Counter/Timer (item 1) Frequency synthesizer (item 2) 50 Ω power splitter (item 21) SMA male-to-BNC female adapter (item 23), three required 50 Ω BNC coaxial cable (item 25), two required N male-to-BNC female adapter (item 27) 50 Ω SMB-to-BNC coaxial cable (item 28) BNC-to-binding post adapter (item 36) Bantam-to-banana plug cable (item 37)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the frequency synthesizer, Universal Counter/Timer, and CTS as shown in Figure 4–12.

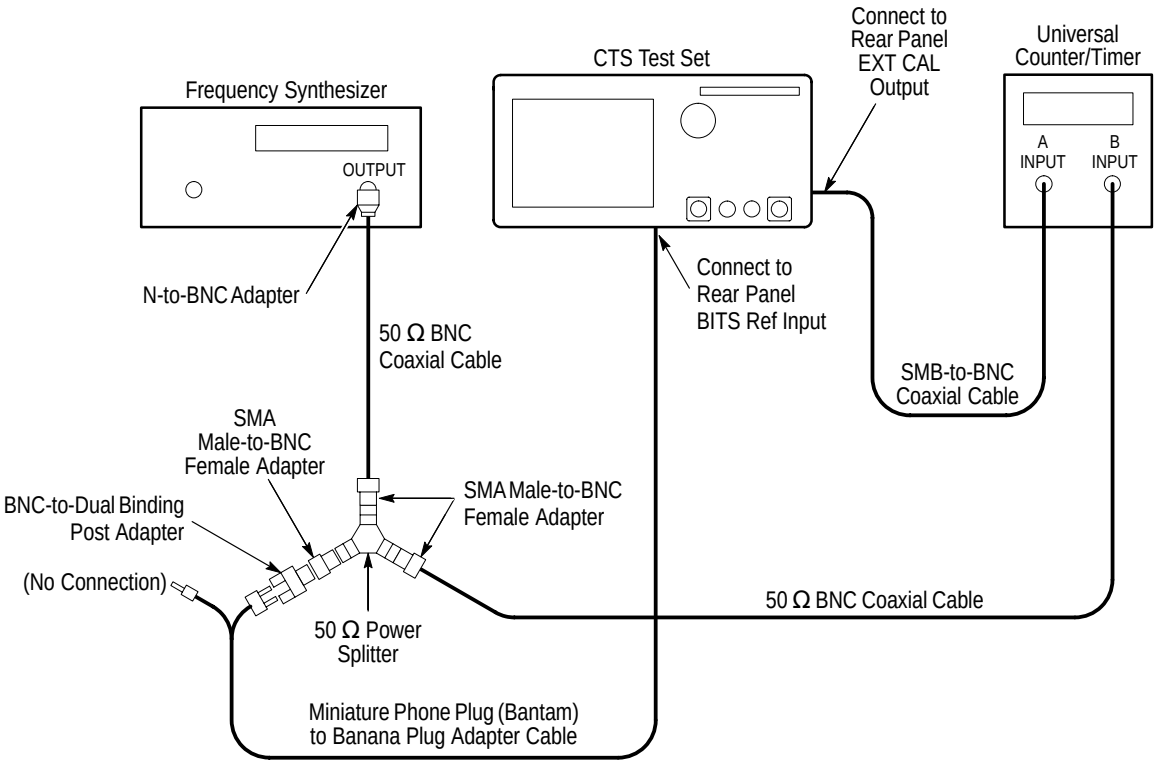

Figure 4–12: BITS Reference Frequency-Lock Hookup

2. Make the following settings on the Universal Counter/Timer:

   a. Set channel A and B input impedance to **50 Ω**.

   b. Set channel A and B input coupling to **AC**.

   c. If you are using a Tektronix DC5010 counter, set the averages to $\mathbf{10^8}$. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the HP53131A/132A Universal Counter operating guide, part number 53131-90021, pages 1-5, 2-7, 2-8, and 2-16, for instructions on how to set **DIGITS**).

   d. Set measurement mode to **Ratio B/A**.

3. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	External BITS

4. Make the following settings on the frequency synthesizer:
   a. Set output frequency to **772,000 Hz**.
   b. Set output power to **+13 dBm** (1 V_{RMS} into 50 Ω).
5. On the Universal Counter/Timer, verify that the frequency ratio reads between 0.014891 and 0.014893 (inclusive).

***NOTE**. If your CTS 710 does not have a tributary add/drop/test option (Option 22), you have completed the performance verification.*

Check Frequency Lock to 2 Mb/s Reference (CTS 750 only)

This test only applies to the CTS 750. If you are testing a CTS 710 without Option 22 installed and have performed all previous functional and physical-layer tests, you have now completed the performance verification.

This test verifies that the transmit clock in the CTS 750 is able to lock to the 2 Mb/s Reference Input. This test measures the frequency ratio of a synthesized 2 Mb/s Reference signal to the transmit clock in order to verify the frequency-locked condition. The transmit clock frequency is measured at the CAL output on the rear panel of the CTS 750.

Equipment Required	Universal Counter/Timer (item 1) Frequency synthesizer (item 2) 50 Ω power splitter (item 21) SMA male-to-BNC female adapter (item 23), three required 50 Ω BNC coaxial cable (item 25), three required N male-to-BNC female adapter (item 27) 50 Ω SMB-to-BNC coaxial cable (item 28)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the frequency synthesizer, Universal Counter/Timer, and CTS as shown in Figure 4–13.

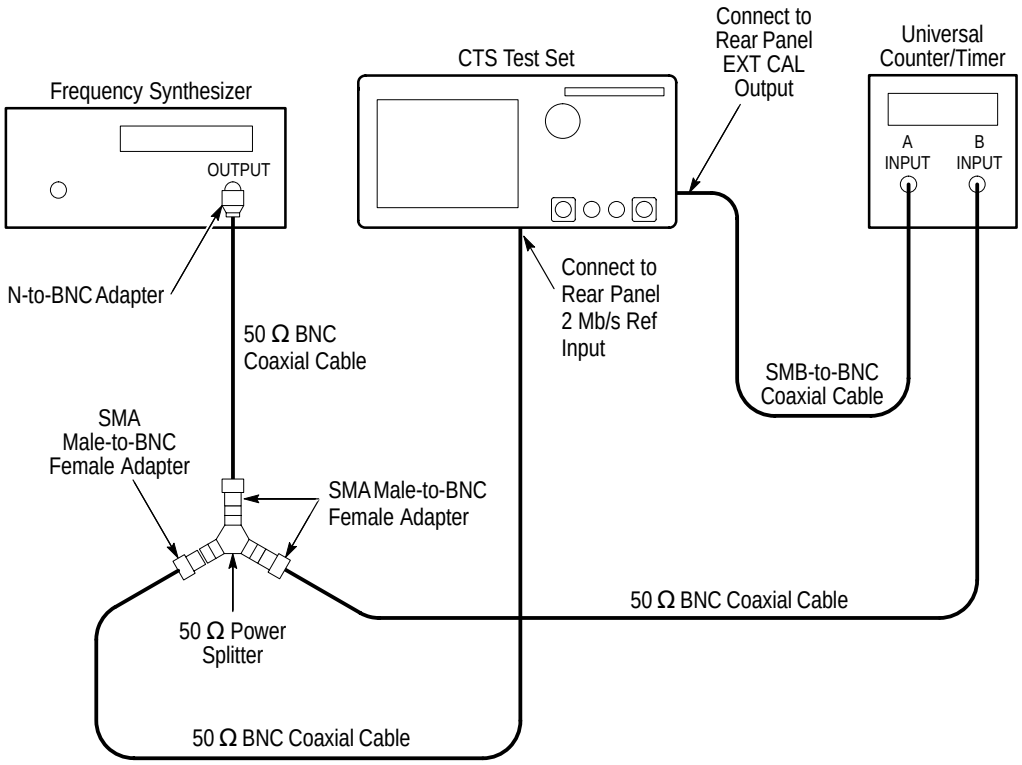

Figure 4–13: 2 Mb/s Reference Frequency-Lock Hookup

2. Make the following settings on the Universal Counter/Timer:

   For the Tektronix DC5010:

   a. Set channel A and B input impedance to **50 Ω**.

   b. Set channel A and B input coupling to **AC**.

   c. Set number of averages to $\mathbf{10^8}$.

   d. Set measurement mode to **Ratio B/A**.

   For the HP53131A:

   e. Set channel 1 and 2 input impedance to **50 Ω**.

   f. Set channel 1 and 2 input coupling to **AC**.

   g. Set **DIGITS** to **8** (refer to the HP53131A/132A Universal Counter operating guide, manual part number 53131-90021, pages 1-5, 2-7, 2-8, and 2-16, for instructions on how to set **DIGITS**).

   h. Set measurement mode to **Ratio 2/1**.

3. Set up the CTS 750 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	External 2 Mb/s

4. Make the following settings on the frequency synthesizer:

   a. Set output frequency to **1.024 MHz**.

   b. Set output power to **+13 dBm** (1 V_{RMS} into 50 Ω).

5. On the Universal Counter/Timer, verify that the frequency ratio reads between 0.019752 and 0.019754 (inclusive).

NOTE. *If your CTS 750 does not have a tributary add/drop/test option (Option 22 or Option 36), you have completed the performance verification.*

Check DS1 Transmit Signal Level (CTS 710 Option 22 only)

This test verifies the signal level from the CTS 710 DS1 output. If you are checking a CTS 750 with Option 36, proceed to *Check 2 Mb/s Balanced Transmit Pulse Mask*, beginning on page 4–76.

Equipment Required	Communications signal analyzer (item 4) 50 Ω SMA coaxial cable (item 22) SMA male-to-BNC female adapter (item 23) 100 Ω Bantam-to-Bantam cable (item 29) Tributary Signal Converter/Attenuator (item 33) 2X Attenuator (item 41), two required
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS1
		Framing	DS1 Unframed
		Test Pattern	1 in 8
		Transmit Line Code	AMI

2. Connect the communications signal analyzer and CTS as shown in Figure 4–14.

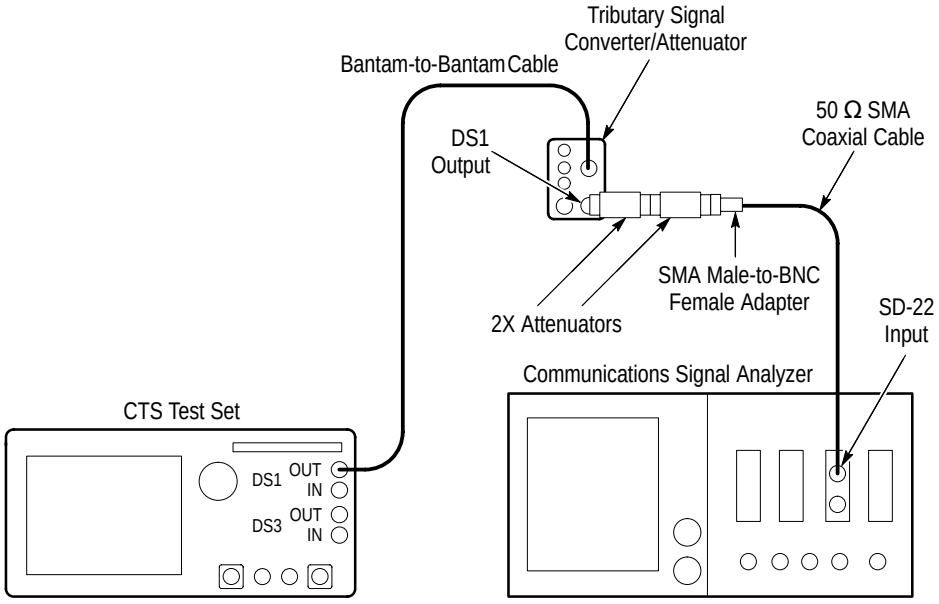

Figure 4–14: DS1 Signal Level Hookup

3. Perform the initial setup of the communications signal analyzer with the following steps:

a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select **Initialize** in the pop-up menu.

b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Select the **Sampling Head Fnc's** pop-up menu.

d. Set the **Ex Channel Attenuation** to 4 $\times$ the calibration factor of the Tributary Signal Converter/Attenuator ($\approx$ 1.6).

e. Select the **TRIGGER** menu. Set the Source to **Internal Clock**.

4. Perform the test with the following sequence on the communications signal analyzer:

a. Press the **AUTOSET** button. The waveform appears untriggered on the communications signal analyzer.

b. Select the **MEASURE** menu and then the **Measurements** pop-up menu.

c. Select the **Peak-peak** measurement, and then select **Exit**.

d. Select the **Peak-peak** measurement selector to display the Peak-peak pop-up menu.

e. Verify that, after 32 acquisitions have completed, the mean value of the peak-peak measurement in the Peak-peak pop-up menu is 6 V ± 1 V.

Check DS1 Transmit Pulse Shape (CTS 710 Option 22 only)

This test verifies the pulse shape of the CTS 710 DS1 output.

Equipment Required	Communications signal analyzer (item 4) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) 100 Ω Bantam-to-Bantam cable (item 29), two required Tributary Signal Converter/Attenuator (item 33) 2X Attenuator (item 41), two required
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–15.

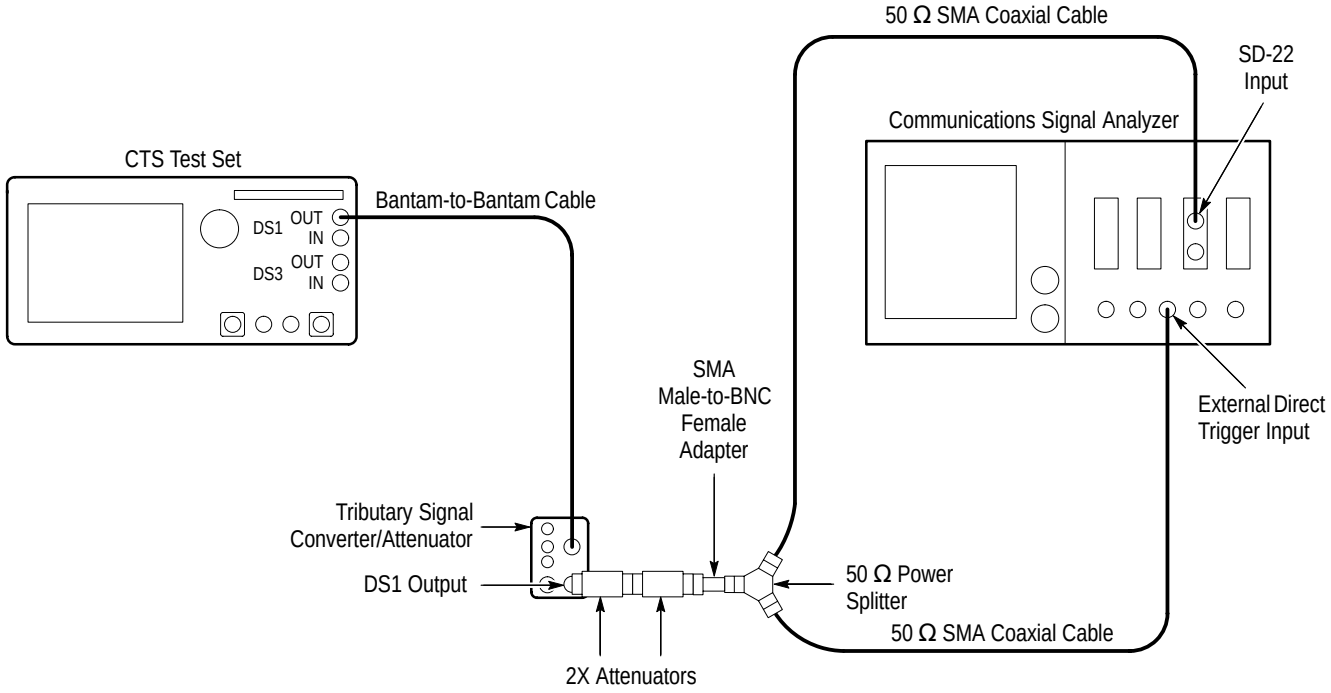

Figure 4–15: DS1 Pulse Shape Hookup

2. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS1
		Test Pattern	1 in 8
		Framing	DS1 Unframed
		Transmit Line Code	AMI

3. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   c. Select the **TRIGGER** menu, set the **Slope** to **+**, and adjust for a stable trigger.

   d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set Average N to **On**.

   e. Select **Set Avg N**, and set Average N to **64**.

   f. Select the **Sampling Head Fnc's** pop-up menu and set **Smoothing** to **On**.

   g. Select the **DISPLAY MODES** menu.

   h. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

   i. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs), and then enter the numeric value **20** followed by **Enter**.

   j. Select the **Standard Masks** pop-up menu and then the **DS1 1.544Mb** menu item from the set of built-in ANSI T1.102 Electrical Standards masks.

4. Perform the test with the following sequence on the communications signal analyzer:

   a. Select the **DISPLAY MODES** menu.

   b. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

   c. Change the **Vertical Offset**, **Vertical Size**, and **Main Position** controls to **Fine** resolution.

   d. Adjust the fine **Vertical Offset**, **Vertical Size**, and **Main Position** controls to position the pulse optimally within the mask.

   e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

   f. Select the **Stop N Waveforms** menu item.

g. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check DS1 Bridged Receive Level (CTS 710 Option 22 only)

This test verifies the DS1 bridged receive level for the CTS DS1 input.

Equipment Required	100 Ω Bantam-to-Bantam Cable (item 29), two required Tributary Signal Converter/Attenuator (item 33), two required 50 Ω terminator (item 42) BNC Male to BNC Male adapter (item 44)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–16.

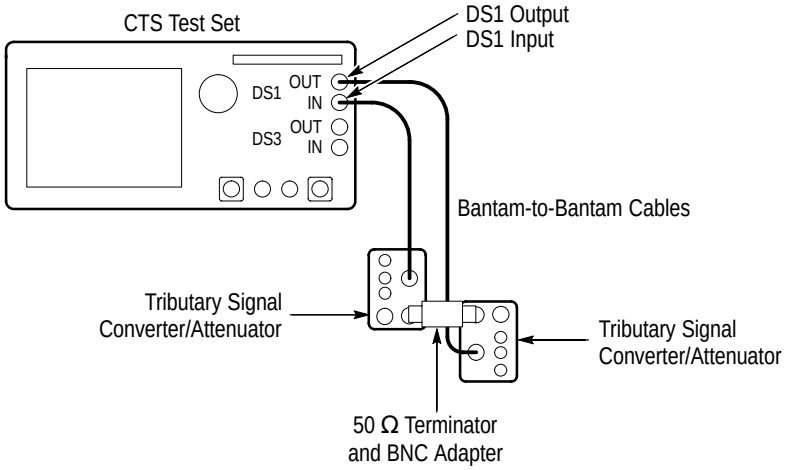

Figure 4–16: DS1 Data Formats Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS1
		Transmit Line Code	B8ZS
		Test Pattern	PRBS2^23–1
		Framing	DS1 Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Cross Connect
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check DS1 Monitor Receive Level (CTS 710 Option 22 only)

This test verifies the monitor receive level of the CTS Option 22 RECEIVE/ADD input.

Equipment Required	Tributary Signal Converter/Attenuator (item 33), two required 100 Ω Bantam-to-Bantam Cable (item 30), two required 10X Attenuator (item 40)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–17.

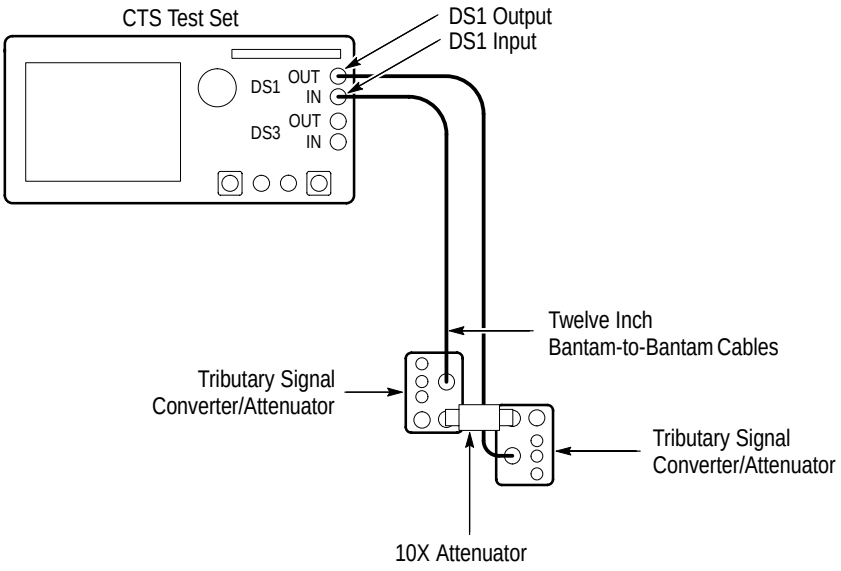

Figure 4–17: DS1 Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS1
		Transmit Line Code	B8ZS
		Test Pattern	PRBS2^23–1
		Framing	DS1 Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Low
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check External Clock Input (CTS 710 Option 22 only)

This test verifies the EXT CLOCK for the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19) 100 Ω Bantam-to-Bantam Cable (item 29), two required
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–18.

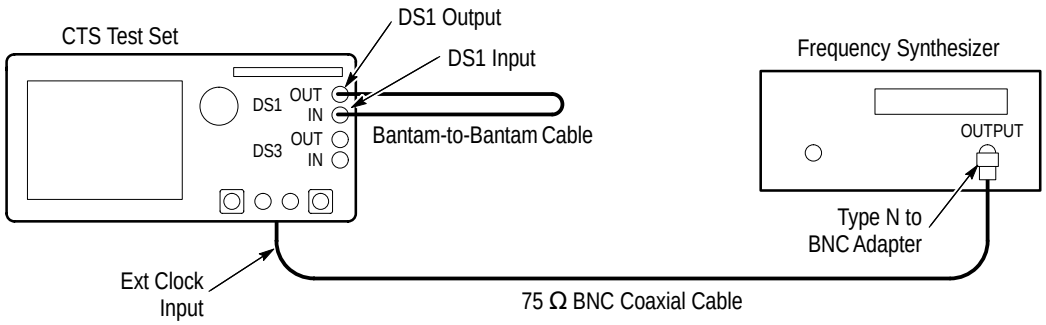

Figure 4–18: DS1 External Clock Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS1
		Transmit Line Code	B8ZS
		Test Pattern	PRBS2^23–1
		Framing	DS1 Unframed
		Transmit Clock	External DSn
RESULTS	MAIN RESULTS	*none*	Errors

3. Make the following settings on the Frequency Synthesizer:

a. Set the output frequency to **1.544231 MHz**.

b. Set the output power to **+4 dBm** ($\approx 1\ V_{p\text{-}p}$ into 50 Ω).

c. Set the RF output to **ON**.

4. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

5. Set the Frequency Synthesizer to **1.543769 MHz**.

6. Perform the test with the following steps:

   a. Press the **START/STOP** button and verify that the START/STOP light is on.

   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

   c. Verify that there are no errors.

   d. Select **Alarms**; verify that there are no alarms.

Check DS3 Transmit Signal Level (CTS 710 Option 22 only)

This test verifies the signal level of the CTS 710 DS3 output.

Equipment Required	Communications signal analyzer (item 4) 75 Ω to 50 Ω Impedance Converter (item 18) 50 Ω SMA coaxial cable (item 22) SMA male-to-BNC female adapter (item 23)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–19.

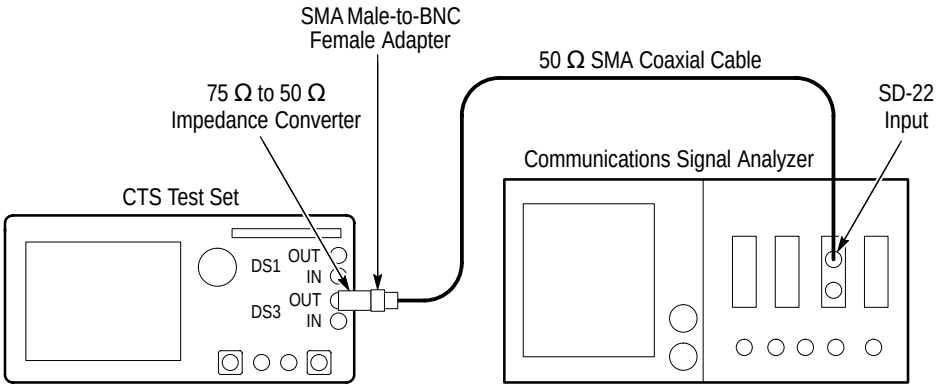

Figure 4–19: DS3 Signal Level Hookup

2. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then **Initialize** in the pop-up menu.

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

   c. Select the **TRIGGER** menu. Set the **Source** to **Internal Clock**.

3. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS3
		Test Pattern	PRBS 2^23–1

4. Perform the test with the following sequence on the communications signal analyzer:

   a. Press the **AUTOSET** button. The waveform appears untriggered on the communications signal analyzer.

   b. Select the **MEASURE** menu and then the **Measurements** pop-up menu.

   c. Select the **Peak-peak** measurement, and then select **Exit**.

   d. Select the **Peak-peak** measurement selector to display the Peak-peak pop-up menu.

   e. Verify that the mean value of the peak-peak measurement in the Peak-peak pop-up menu is between 0.29 V and 0.55 V.

Check DS3 Pulse Shape (CTS 710 Option 22 only)

This test verifies the pulse shape from the CTS 710 DS3 output.

Equipment Required	Communications signal analyzer (item 4) Filter (item 8) 75 Ω to 50 Ω impedance converter (item 18) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–20.

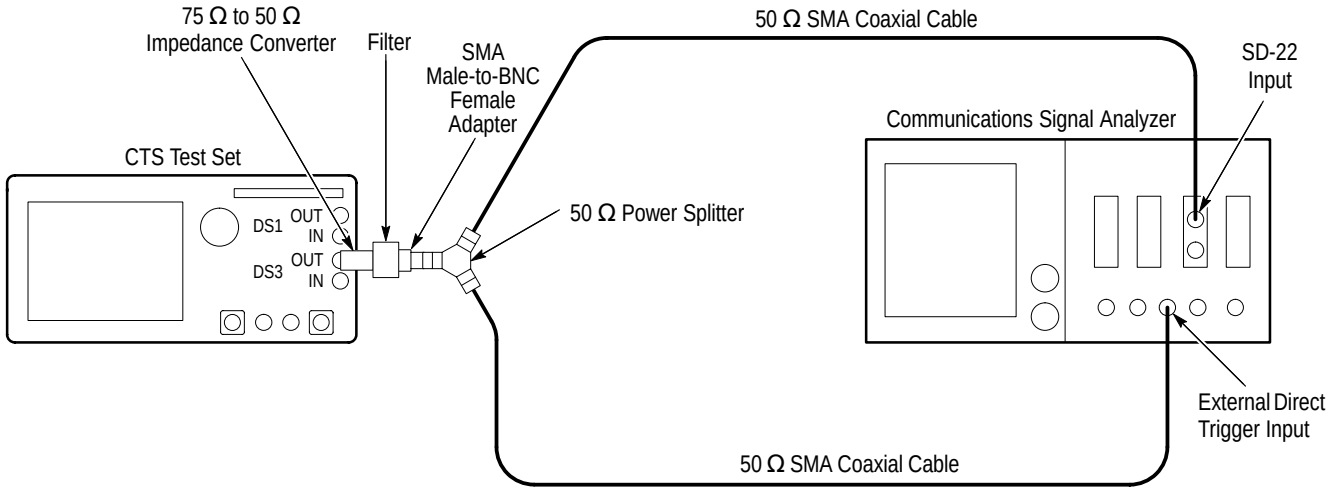

Figure 4–20: DS3 Pulse Shape Hookup

2. Set up the CTS 710 with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS3
		Test Pattern	User Word 24 bit
			Default 100100100 100100100100100

3. Perform the initial setup of the communications signal analyzer with the following steps:

a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Select the **TRIGGER** menu, set the **Slope** to **+**, and **Level** to **20 mV**.

d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set Average N to **On**.

e. Select the **Sampling Head Fnc's** pop-up menu and set **Smoothing** to **On**.

f. Select the **DISPLAY MODES** menu.

g. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

h. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs) then enter the numeric value **20** followed by **Enter**.

i. Select the **Standard Masks** pop-up menu and then the **DS3 44.736Mb** menu item from the set of built-in ANSI T1.102 Electrical Standards masks.

4. Perform the test with the following sequence on the communications signal analyzer:

   a. If necessary, select the **DISPLAY MODES** menu.

   b. Press **AUTOSET**.

   c. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

   d. Change the **Vertical Offset**, **Vertical Size**, and **Main Position** controls to **Fine** resolution.

   e. Adjust the fine **Vertical Offset**, **Vertical Size**, and **Main Position** controls to position the pulse optimally within the mask.

   f. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

   g. Select the **Stop N Waveforms** menu item.

   h. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

   i. Remove the displayed input trace.

   j. Select **Define Trace**.

   k. Define the trace as **–M1** (this assumes the input signal is connected to M1).

   l. Select the **DISPLAY MODES** menu.

   m. Select the **Standard Masks** pop-up menu and then the **DS3 44.736Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

   n. Press **AUTOSET**.

   o. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

   p. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

   q. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

r. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

s. Select the **Stop N Waveforms** menu item.

t. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check DS3 Monitor Receive Level (CTS 710 Option 22 only)

This test verifies the monitor receive level of the CTS DS3 input.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required BNC Female to BNC Female adapter (item 26) 10X Attenuator (item 38)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–21.

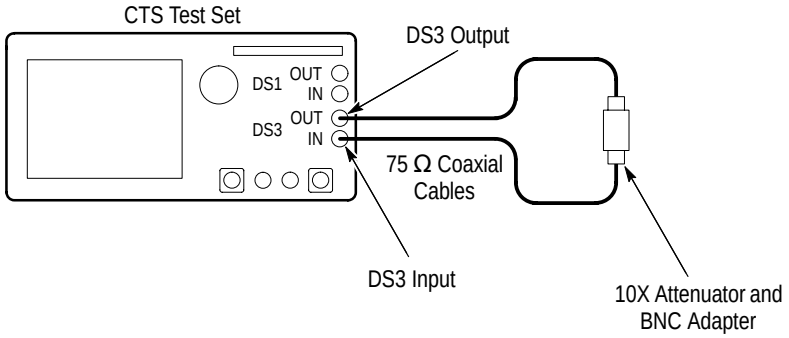

Figure 4–21: DS3 Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS3
		Test Pattern	User Word 8 bit
			Default 10101010
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check External Clock Input (CTS 710 Option 22 only)

This test verifies the EXTERNAL CLOCK input of the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19), two required N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–22.

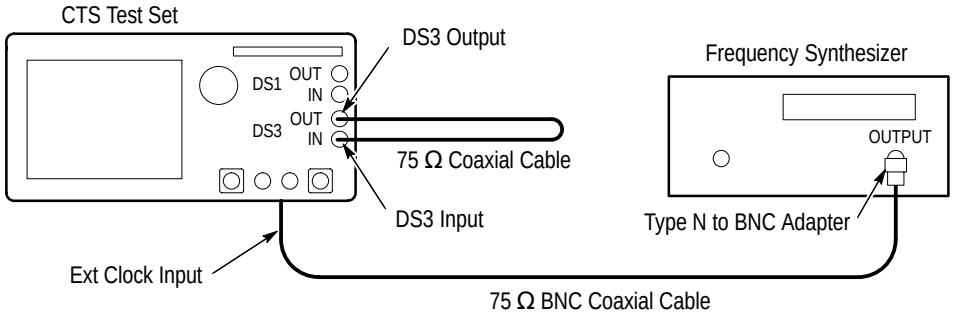

Figure 4–22: DS3 External Clock Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	DS3
		Test Pattern	PRBS2^23–1
		Framing	DS3 Unframed
		Transmit Clock	External DSn
RESULTS	MAIN RESULTS	*none*	Errors

3. Make the following settings on the Frequency Synthesizer:

a. Set the output frequency to **44.742710 MHz**.

b. Set the output power to **+4 dBm** ($\approx$1 $V_{p\text{-}p}$ into 50 Ω).

c. Set the RF output to **ON**.

4. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

5. Set the Frequency Synthesizer to **44.729290 MHz**.

6. Perform the test with the following steps:

   a. Press the **START/STOP** button and verify that the START/STOP light is on.

   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

   c. Verify that there are no errors.

   d. Select **Alarms**; verify that there are no alarms.

***NOTE**. If you have performed all previous functional and physical-layer tests that are applicable to your CTS, you have now completed the performance verification.*

Check 2 Mb/s Balanced Transmit Pulse Mask (CTS 750 Option 36 only)

This test verifies the pulse mask from the CTS 2 Mb/s output.

Equipment Required	Communications signal analyzer (item 4) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) Tributary Signal Converter/Attenuator (item 33) 120 Ω DIN41628L cable (item 35) 2X Attenuator (item 41), two required
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–23.

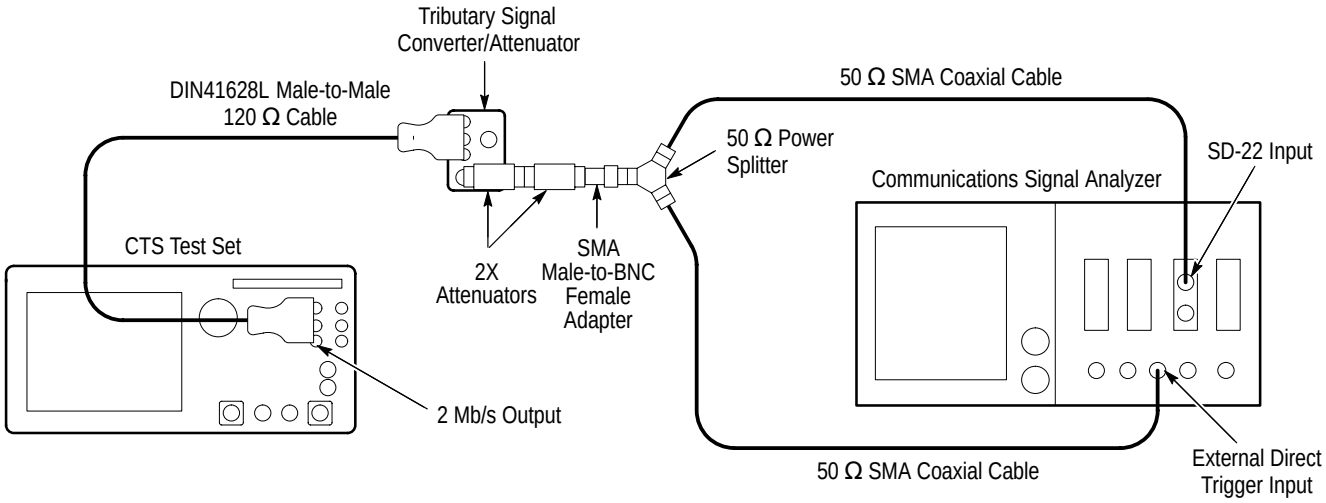

Figure 4–23: 2 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Balanced
		Test Pattern	All Ones
		Framing	2 Mb/s Unframed
		Transmit Clock	Internal

3. Perform the initial setup of the communications signal analyzer with the following steps:

a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Adjust for 200 ns/DIV, 200 mV/DIV, and a stable trigger (if necessary, select the trigger menu, and adjust the Trigger Level for a stable trigger).

d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

e. Select **Set Avg N**, and set **Average N** to **64**.

f. Select the **Sampling Head Fnc's** pop-up menu.

g. Set the **Ex Channel Attenuation** to 8 × the calibration factor of the Tributary Signal Converter/Attenuator.

h. Select the **DISPLAY MODES** menu.

i. Set the **Vertical Size** to **525 mV/DIV**.

j. Select **Mask Testing** pop-up menu, then select the **Set N Waveforms** menu item, then press **Exit**.

k. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs), and then enter the numeric value **20** followed by **Enter**.

4. Perform the test with the following sequence on the communications signal analyzer:

a. Select the **DISPLAY MODES** menu.

b. Select the **Standard Masks** pop-up menu and then the **Sym. Pair 2.048Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

c. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

d. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

e. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

f. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

g. Select the **Stop N Waveforms** menu item.

h. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

i. Remove the displayed input trace.

j. Select **Define Trace** (in the upper right-hand corner of the CSA-803 screen).

k. Define the trace as **–M1** (this assumes the input signal is connected to M1) by pressing the **-** keypad key, then **Mainframe channels 1**, then **Enter Desc**.

l. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, set **Average N** to **On**, then press **Exit**.

m. Verify that the V/DIV display and sampling head Ex Channel Attenuation have not changed.

n. Select the **DISPLAY MODES** menu.

o. Select the **Standard Masks** pop-up menu and then the **Sym. Pair 2.048Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

p. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

q. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

r. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

s. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

t. Select the **Stop N Waveforms** menu item.

u. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check 2 Mb/s Monitor Receive Level (CTS 750 Option 36 only)

This test verifies the monitor receive level for the CTS Option 36 RECEIVE/ADD input.

Equipment Required	Tributary Signal Converter/Attenuator (item 33), two required 10X Attenuator (item 40) 2X Attenuator (item 41) 120 Ω DIN41628L cable (item 34), two required BNC Male to BNC Male Adapter (item 44)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–24.

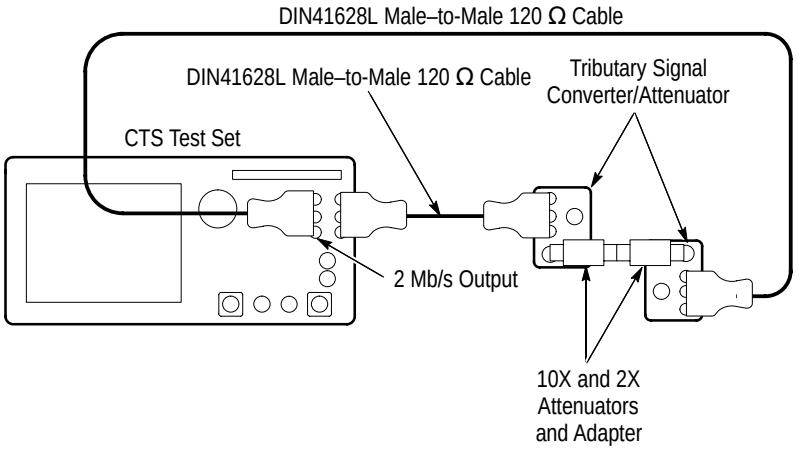

Figure 4–24: 2 Mb/s Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Balanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check the 2 Mb/s Balanced Bridged Receive Level (CTS 750 Option 36 only)

This test verifies the bridged receive level for the CTS 2 Mb/s input.

Equipment Required	Tributary Signal Converter/Attenuator (item 33), two required 50 Ω BNC cable (item 25) 120 Ω DIN41628L cable (item 34), two required 50 Ω terminator (item 42)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–25.

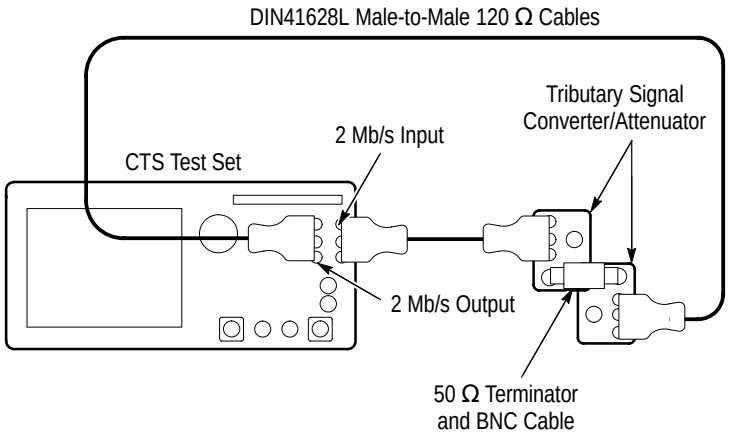

Figure 4–25: 2 Mb/s Bridged Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Balanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Bridge
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check 2 Mb/s Balanced External Clock Input (CTS 750 Option 36 only)

This test verifies the external Clock input of the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19) N-to-BNC adapter (item 27) 120 Ω DIN41628L cable (item 34)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–26.

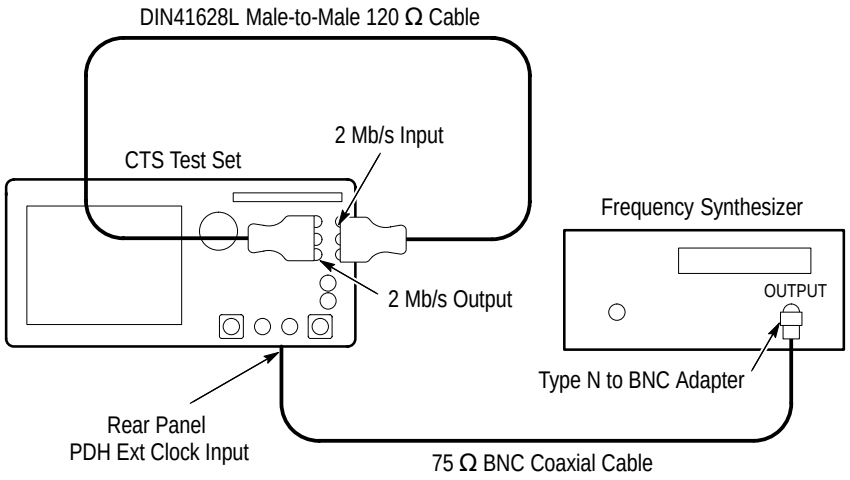

Figure 4–26: 2 Mb/s External Clock Hookup

2. Make the following settings on the Frequency Synthesizer:

- **a.** Set the output frequency to **2.048307 MHz**.
- **b.** Set the output power to **+4 dBm** ($\approx 1\ V_{p\text{-}p}$ into 50 Ω).
- **c.** Set the RF output to **ON**.

3. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Balanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
		Transmit Clock	External PDH
RESULTS	MAIN RESULTS	*none*	Errors

4. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

5. Set the Frequency Synthesizer to **2.047693 MHz**.

6. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

Check the 2 Mb/s Unbalanced Transmit Pulse Mask (CTS 750 Option 36 only)

This test verifies the 2 Mb/s pulse mask from the CTS.

Equipment Required	Communications signal analyzer (item 4) 75 Ω to 50 Ω impedance converter (item 18) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) 50 Ω coaxial cable (item 25) 2X Attenuator (item 41)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–27.

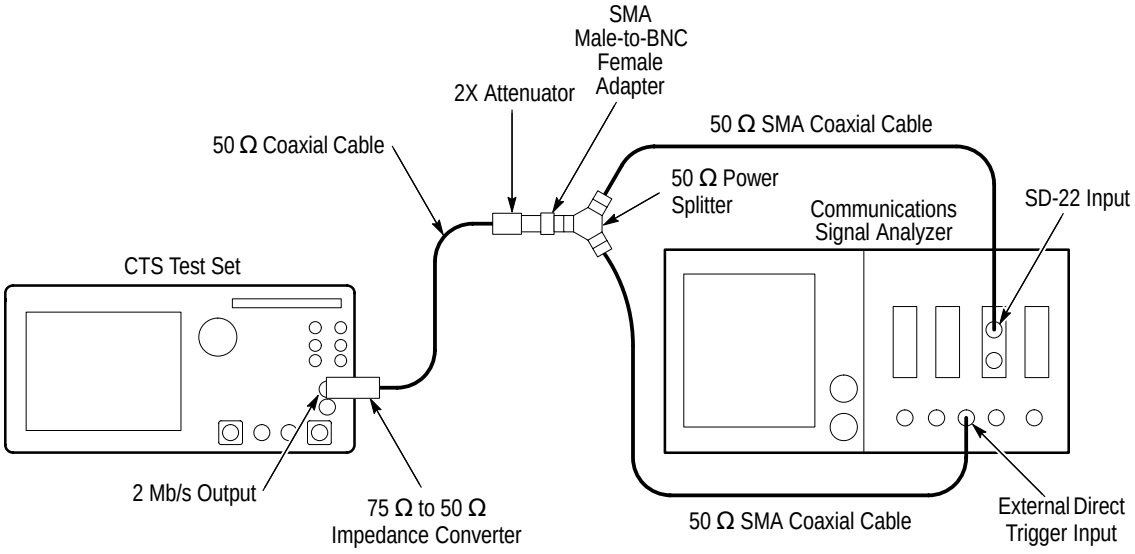

Figure 4–27: 2 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Unbalanced
		Test Pattern	All Ones
		Framing	2 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the initial setup of the communications signal analyzer with the following steps:

a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Adjust the communications signal analyzer for 200 ns/div, 200 mV/div, and a stable trigger.

d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

e. Select **Set Avg N**, and set **Average N** to **64**.

f. Select the **Sampling Head Fnc's** pop-up menu.

g. Set the **Ex Channel Attenuation** to **9.6**.

h. Select the **DISPLAY MODES** menu.

i. Select the **Standard Masks** pop-up menu and then the **CoAx Pair 2.048Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

j. Set the **Vertical Size** to **414 mV/DIV**.

k. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

l. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs) then enter the numeric value **20** followed by **Exit**.

4. Perform the test with the following sequence on the communications signal analyzer:

a. Select the **DISPLAY MODES** menu.

b. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

c. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

d. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

g. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

h. Remove the displayed input trace.

i. Select **Define Trace**.

j. Define the trace as **–M1** (this assumes the input signal is connected to M1).

k. Verify that the V/DIV display and the sampling head Ex Channel Attenuation have not changed.

l. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

m. Select the **DISPLAY MODES** menu.

n. Select the **Standard Masks** pop-up menu and then the **CoAx Pair 2.048Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

o. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

p. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

q. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

r. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

s. Select the **Stop N Waveforms** menu item.

t. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check the 34 Mb/s Unbalanced Transmit Pulse Mask (CTS 750 Option 36 only)

This test verifies the 34 Mb/s pulse mask from the CTS.

Equipment Required	Communications signal analyzer (item 4) 75 Ω to 50 Ω impedance converter (item 18) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) 50 Ω coaxial cable (item 25)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–28.

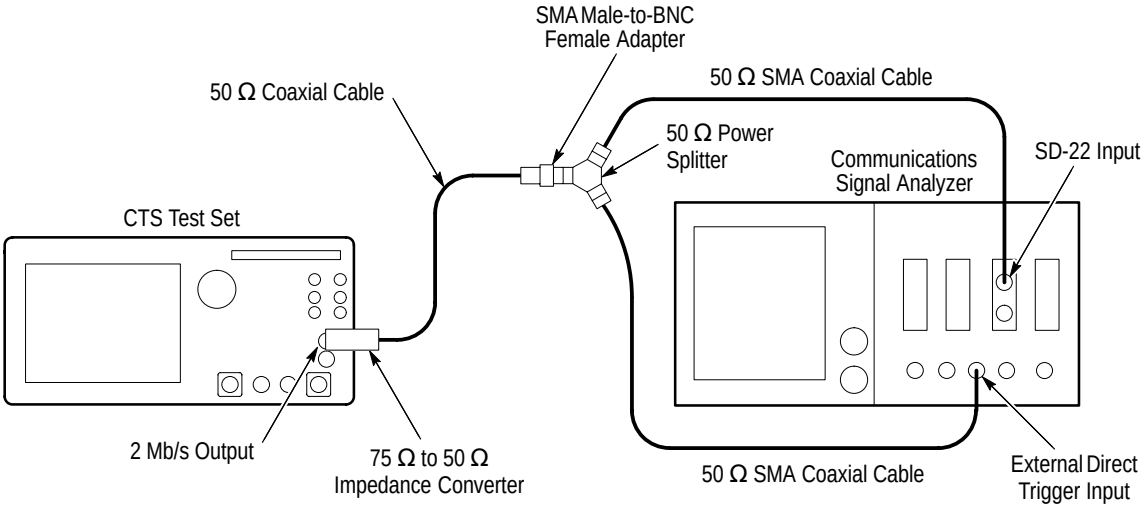

Figure 4–28: 34 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s
		Test Pattern	All Ones
		Framing	34 Mb/s Unframed

3. Perform the initial setup of the communications signal analyzer with the following steps:

a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Adjust the communications signal analyzer for 10 ns/DIV, 50 mV/DIV, and a stable trigger.

d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

e. Select **Set Avg N**, and set **Average N** to **64**.

f. Select the **Sampling Head Fnc's** pop-up menu and set **Smoothing** to **On**.

g. Set the **Ex Channel Attenuation** to **4.8**.

h. Select the **DISPLAY MODES** menu.

i. Select the **Standard Masks** pop-up menu and then the **Pulse 34.368Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

j. Set the **Vertical Size** to **175 mV/DIV** (use the setting closest to 175 mV).

k. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

l. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs) then enter the numeric value **20** followed by **Exit**.

4. Perform the test with the following sequence on the communications signal analyzer:

a. Select the **DISPLAY MODES** menu.

b. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

c. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

d. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

g. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

h. Remove the displayed input trace.

i. Select **Define Trace**.

j. Define the trace as **–M1** (this assumes the input signal is connected to M1).

k. Verify that the V/DIV display and sampling head Ex Channel Attenuation have not changed.

l. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

m. Select the **DISPLAY MODES** menu.

n. Select the **Standard Masks** pop-up menu and then the **Pulse 34.368Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

o. Adjust **Vertical Offset** and **Main Position** to locate a positive-going pulse at the center of the mask.

p. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

q. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

r. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

s. Select the **Stop N Waveforms** menu item.

t. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check the 140 Mb/s Unbalanced Transmit Pulse Mask (CTS 750 Option 36 only)

This test verifies the 140 Mb/s pulse mask from the CTS.

Equipment Required	Communications signal analyzer (item 4) 75 Ω to 50 Ω impedance converter (item 18) 50 Ω power splitter (item 21) 50 Ω SMA coaxial cable (item 22), two required SMA male-to-BNC female adapter (item 23) 50 Ω coaxial cable (item 25)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4–29.

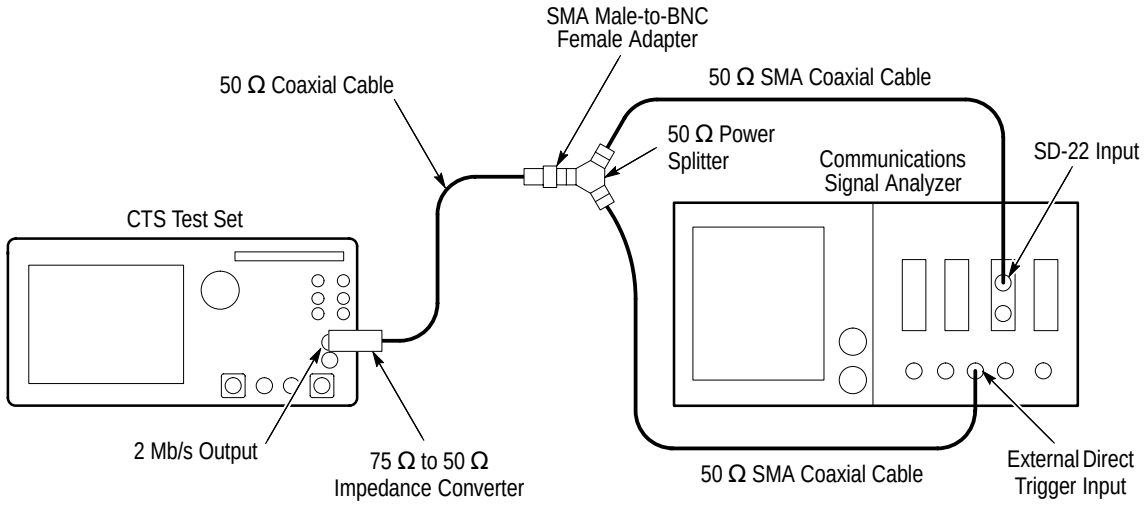

Figure 4–29: 140 Mb/s Transmit Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	All Ones
		Framing	140 Mb/s Unframed

3. Perform the initial setup of the communications signal analyzer with the following steps:

   a. To initialize the communications signal analyzer, select the **UTILITY** menu, the **Initialize** pop-up menu, and then select the **Initialize** menu item in the pop-up menu.

   b. Press the **SELECT CHANNEL** button next to the input connector on the sampling head channel you are using.

c. Adjust the communications signal analyzer for 10 ns, 50 mV, and a stable trigger.

d. Select the **WAVEFORM** menu, select the **Acquire Desc** pop-up menu, and set **Average N** to **On**.

e. Select **Set Avg N**, and set **Average N** to **64**.

f. Select the **Sampling Head Fnc's** pop-up menu.

g. Set the **Ex Channel Attenuation** to **4.8**.

h. Select the **DISPLAY MODES** menu.

i. Select the **Standard Masks** pop-up menu and then the **One Pulse 139.26 Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

j. Set the **Vertical Size** to **143 mV/DIV** (use the setting closest to 143 mV).

k. Select **Mask Testing** pop-up menu and then the **Set N Waveforms** menu item.

l. Select the **Waveform N** pop-up menu (red boxes located just to the left of the two front panel knobs) then enter the numeric value **20** followed by **Exit**.

4. Perform the test with the following sequence on the communications signal analyzer:

a. Select the **DISPLAY MODES** menu.

b. Adjust **Vertical Offset** and **Main Position** to locate the waveform at the center of the mask.

c. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

d. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

g. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

h. On the communications signal analyzer, select the **Standard Masks** pop-up menu and then the **Zero Pulse 139.26 Mb** menu item from the set of built-in ITU G.703 Electrical Standards masks.

5. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	All Zeros
		Framing	140 Mb/s Unframed

6. Perform the test with the following sequence on the communications signal analyzer:

a. Select the **DISPLAY MODES** menu.

b. Adjust **Vertical Offset** and **Main Position** to locate the waveform at the center of the mask.

c. Change the **Vertical Offset** and **Main Position** controls to **Fine** resolution.

d. Adjust the fine **Vertical Offset** and **Main Position** controls to position the pulse optimally within the mask.

e. Select the **Mask Testing** pop-up menu and then the **Pass/Fail Test** menu item.

f. Select the **Stop N Waveforms** menu item.

g. After 20 waveforms have been acquired, the acquisition stops automatically. Verify that the test has passed, which is indicated by the green Passing message displayed in the Mask Testing pop-up menu selector.

Check the 2 Mb/s Unbalanced Bridged Receive Level (CTS 750 Option 36 only)

This test verifies the bridged receive level of the CTS 2 Mb/s input.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required BNC Female to BNC Female adapter (item 26) 75 Ω terminator (item 43)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–30.

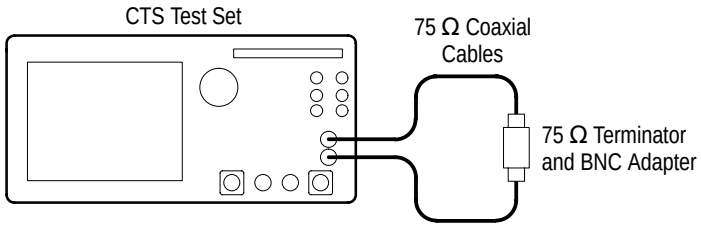

Figure 4–30: 2 Mb/s Bridged Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Unbalanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Bridge
RESULTS	MAIN RESULTS	*none*	Errors

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **Alarms**; verify that there are no alarms.

e. Select **Failures**; verify that there are no failures.

Check the 2 Mb/s Unbalanced Monitor Receive Level (CTS 750 Option 36 only)

This test verifies the 2 Mb/s monitor receive level of the CTS.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required BNC Female to BNC Female adapter (item 26) 10X Attenuator (item 38) 2X Attenuator (item 39)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–31.

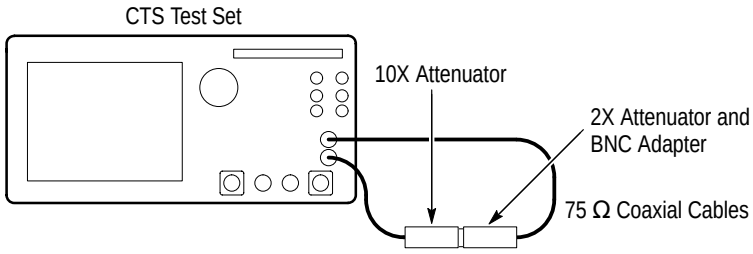

Figure 4–31: 2 Mb/s Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Unbalanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Check the 34 Mb/s Monitor Receive Level (CTS 750 Option 36 only)

This test verifies the 34 Mb/s monitor receive level of the CTS.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required BNC Female to BNC Female adapter (item 26) 10X attenuator (item 38) 2X attenuator (item 39)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–32.

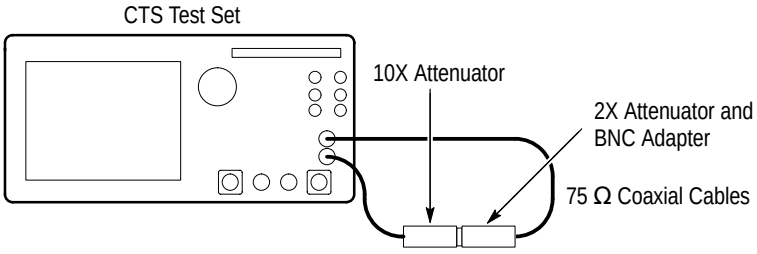

Figure 4–32: 34 Mb/s Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

3. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Check the 140 Mb/s Monitor Receive Level (CTS 750 Option 36 only)

This test verifies the 140 Mb/s monitor receive level for the CTS.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required BNC Female to BNC Female adapter (item 26) 10X attenuator (item 38) 2X attenuator (item 39)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–33.

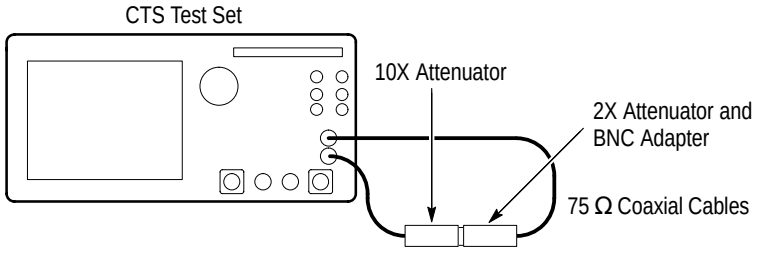

Figure 4–33: 140 Mb/s Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	140 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

3. Press the **START/STOP** button: verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Check the 2 Mb/s Unbalanced External Clock input (CTS 750 Option 36 only)

This test verifies the 2 Mb/s external clock input of the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19), two required N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–34.

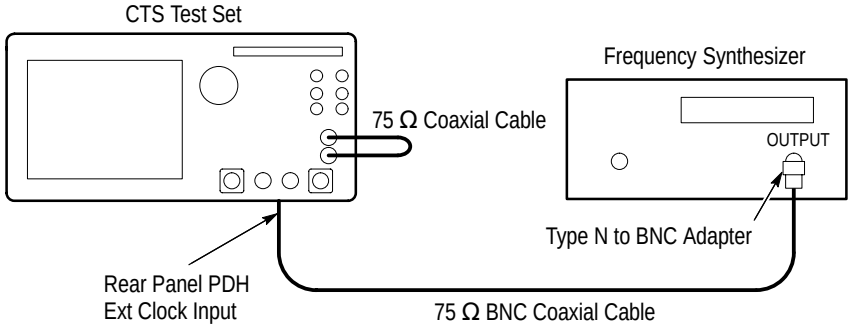

Figure 4–34: 2 Mb/s External Clock Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s Unbalanced
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
		Transmit Clock	External 2 Mb/s
RESULTS	MAIN RESULTS	*none*	Errors

3. Make the following settings on the Frequency Synthesizer:

a. Set the output frequency to **2.048307 MHz**.

b. Set the output power to **+4 dBm** ($\approx$1 $V_{p\text{-}p}$ into 50 Ω).

c. Set the RF output to **ON**.

4. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.
5. Set the Frequency Synthesizer to **2.047693 MHz**.
6. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.

Check the 34 Mb/s External Clock input (CTS 750 with Option 36 but no Option 14 only)

This test verifies the 34 Mb/s external clock input of the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19), two required N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–35.

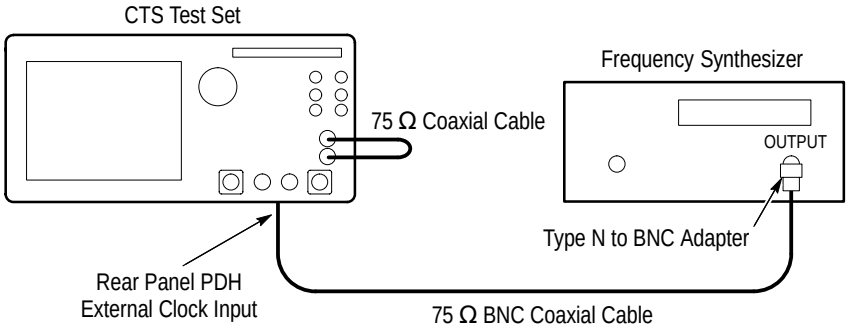

Figure 4–35: 34 Mb/s External Clock Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	34 Mb/s Unframed
		Transmit Clock	External PDH
RESULTS	MAIN RESULTS	*none*	Errors

3. Make the following settings on the Frequency Synthesizer:

a. Set the output frequency to **34.373155 MHz**.

b. Set the output power to **+4 dBm** ($\approx$1 $V_{p\text{-}p}$ into 50 Ω).

c. Set the RF output to **ON**.

4. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.
5. Set the Frequency Synthesizer to **34.362845 MHz**.
6. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.

Check the 140 Mb/s External Clock input (CTS 750 with Option 36 but no Option 14 only)

This test verifies the 140 Mb/s external clock input of the CTS.

Equipment Required	Frequency Synthesizer (item 2) 75 Ω BNC coaxial cable (item 19), two required N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–36.

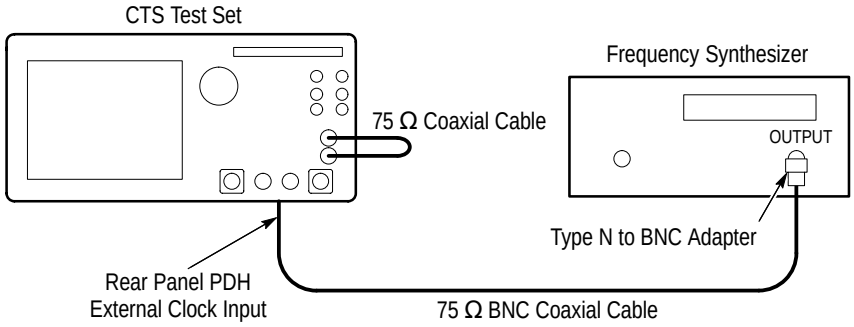

Figure 4–36: 140 Mb/s External Clock Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	140 Mb/s Unframed
		Transmit Clock	PDH External
RESULTS	MAIN RESULTS	*none*	Errors

3. Make the following settings on the Frequency Synthesizer:

a. Set the output frequency to **278.569779 MHz**.

b. Set the output power to **+4 dBm** ($\approx$1 $V_{p\text{-}p}$ into 50 Ω).

c. Set the RF output to **ON**.

4. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.
5. Set the Frequency Synthesizer to **278.486221 MHz**.
6. Perform the test with the following steps:
   a. Press the **START/STOP** button and verify that the START/STOP light is on.
   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.
   c. Verify that there are no errors.
   d. Select **Alarms**; verify that there are no alarms.

Check the 2 Mb/s Balanced Cable Equalization (CTS 750 Option 36 only)

This test verifies the 2 Mb/s cable equalization of the CTS.

Equipment Required	2 Mb/s Signal Source (item 5) 120 Ω DIN41628L cable (item 34)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–37.

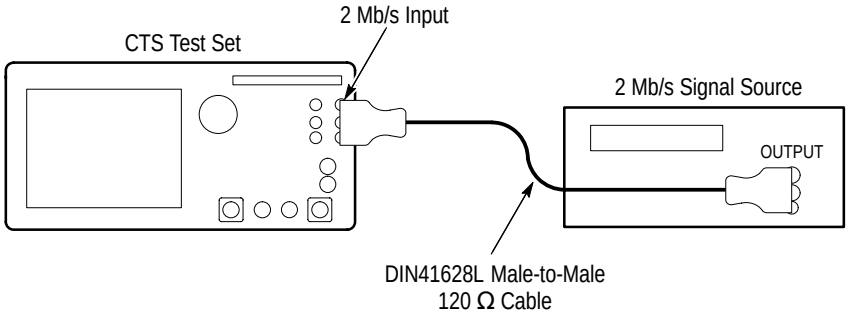

Figure 4–37: 2 Mb/s Cable Equalization Hookup

2. Perform the initial setup of the 2 Mb/s Signal Source with the following steps:

a. Set the 2 Mb/s Signal Source to output a 2 Mb/s balanced, PRBS2^23–1 unframed signal.

3. Set up the CTS (underr test)with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
RECEIVE	RECEIVE SETTINGS	Receive Rate	2 Mb/s Balanced
		Receive Level	Normal
		Test Pattern	PRBS 2^23–1
		Framing	2 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	Errors

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Check the 34 Mb/s Cable Equalization (CTS 750 Option 36 only)

This test verifies the 34 Mb/s Cable Equalization for the CTS.

Equipment Required	656 ft (200 m) length of 75 Ω Reference Cable (items 13, 14, and 17 connected in series)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–38.

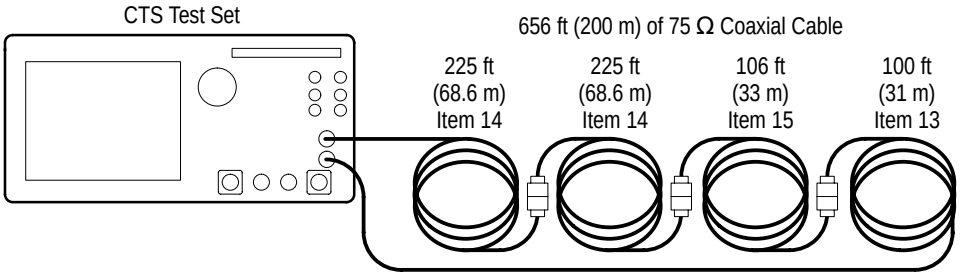

Figure 4–38: 34 Mb/s Cable Equalization Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Normal
RESULTS	MAIN RESULTS	*none*	Errors

3. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Check the 140 Mb/s Cable Equalization (CTS 750 Option 36 only)

This test verifies the 140 Mb/s Cable Equalization for the CTS.

Equipment Required	656 ft (200 m) length of 75 Ω Reference Cable (items 13, 14, and 17 connected in series)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4–39.

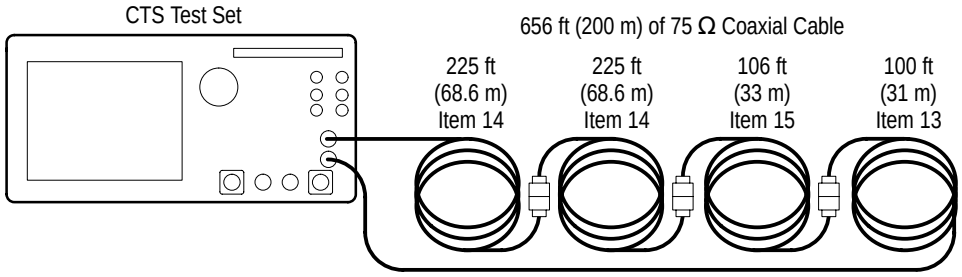

Figure 4–39: 140 Mb/s Cable Equalization Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23–1
		Framing	140 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Normal
RESULTS	MAIN RESULTS	*none*	Errors

3. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Low-Frequency Jitter Tests (CTS 750 Option 14 only)

Perform the following setup to prepare for the Low-Frequency Jitter Tests.

Equipment Required	75 Ω BNC coaxial cable (item 19), two required Optical fiber cable (item 13)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately 30 minutes

1. Connect the CTS inputs and outputs in a loop-back configuration as shown in Figure 4–40.

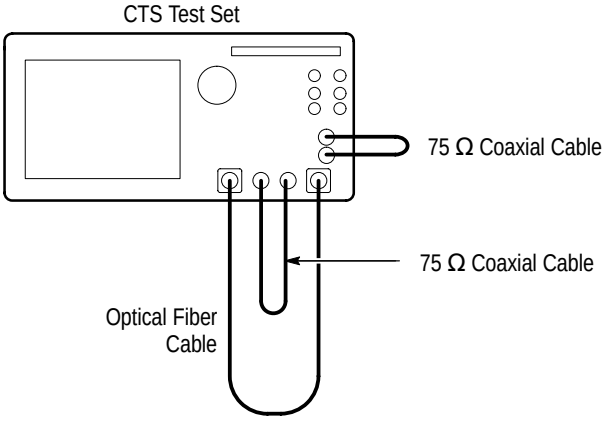

Figure 4–40: Low-Frequency Jitter Test Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On
		Jitter Output	Line
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

3. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

NOTE*. In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. Table 4–5 describes the specific conditions for each test. You will repeat the process for each row in Table 4–5.*

4. For each row in Table 4–5, setup the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Frequency	*as specified in column 1 of Table 4–5* *
		Jitter Amplitude	*as specified in column 2 of Table 4–5* *
RECEIVE	JITTER & WANDER	Jitter Measurement Range	*as specified in column 3 of Table 4–5*
		Jitter Input Filter	*as specified in column 4 of Table 4–5*
		Fullband Highpass	*as specified in column 5 of Table 4–5*
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	*as specified in column 6 of Table 4–5*
RESULTS	MAIN RESULTS	*none*	Jitter/Wander

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

5. Press the **START/STOP** button, and verify that the START/STOP light is on.
6. Wait 30 seconds for the test to complete.
7. Verify that the current peak-to-peak jitter measurement is within the limits specified in column 7 of Table 4–5 (inclusive).
8. Repeat steps 4 through 7 for each row in Table 4–5.

Table 4–5: Low-Frequency Jitter Tests

Jitter Frequency	Jitter Amplitude	Jitter Range	Jitter Filter	Fullband Highpass	Transmit Rate	Test Limits
15 Hz	200 UI	Extended	Fullband	1 Hz	2 Mb/s (Unbalanced)	189.25 to 209.87 UI
15 Hz	200 UI	Extended	Fullband	1 Hz	34 Mb/s	189.35 to 209.77 UI
15 Hz	200 UI	Extended	Fullband	1 Hz	140 Mb/s	189.35 to 209.77 UI
15 Hz	200 UI	Extended	Fullband	1 Hz	STM-0E	189.35 to 209.77 UI
15 Hz	200 UI	Extended	Fullband	1 Hz	STM-1E	189.35 to 209.77 UI
15 Hz	200 UI	Extended	Fullband	1 Hz	STM-4	188.80 to 210.32 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	2 Mb/s (Unbalanced)	14.95 to 16.97 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	34 Mb/s	15.05 to 16.87 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	140 Mb/s	15.05 to 16.87 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	STM-0E	15.05 to 16.87 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	STM-1E	15.05 to 16.87 UI
150 Hz	16 UI	Extended	Fullband	10 Hz	STM-4	14.90 to 17.02 UI

High-Amplitude Jitter Tests (CTS 750 Option 14 only)

Perform the following setup to prepare for the High-Amplitude Jitter Tests.

Equipment Required	Spectrum analyzer (item 12) 75 Ω BNC coaxial cable (item 19), three required Optical fiber cable (item 13) 75 Ω to 50 Ω impedance converter (item 18) N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately 90 minutes

1. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

2. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

CAUTION. *To prevent damage to the spectrum analyzer, follow the next step carefully before completing the instrument hookup.*

3. Perform the initial setup of the spectrum analyzer with the following steps:

   a. Set the reference level to **0 dBm**.

   b. Set the vertical scale factor to **10 dB/division**.

   c. Set the sweep to **free run**.

   d. Set the sweep to **auto** (or **coupled**).

4. Connect the CTS inputs and outputs in a loop-back configuration. Also, connect the rear-panel jitter clock output (J/CLK) to the spectrum analyzer RF input as shown in Figure 4–41.

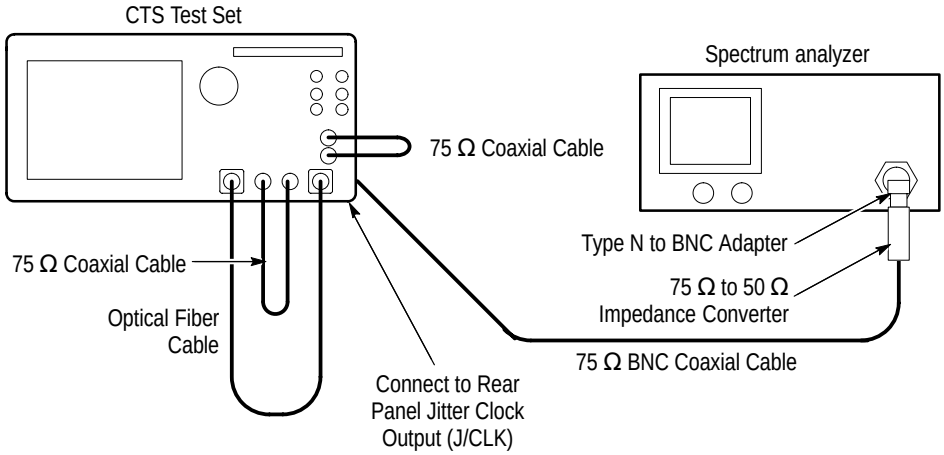

Figure 4–41: High Amplitude Jitter Test Hookup

***NOTE**. In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. The three tables that follow describe the specific conditions for each test. You will repeat the process for each row in the tables.*

5. For each row in Table 4–6, set up the spectrum analyzer as follows:

   a. Set the span (total over 10 divisions) to the value in column 3 of Table 4–6.

   b. Set both the resolution bandwidth and video bandwidth to the value in column 4 of Table 4–6.

   c. Set the center frequency to the value in column 5 of Table 4–6.

Table 4–6: Spectrum Analyzer Setups

Transmit/Clock Rate	Jitter Frequency	Ten-Division Span	Resolution Bandwidth and Video Bandwidth	Center Frequency
2 Mb/s (Unbalanced)	2.5 kHz	10 kHz	300 Hz	2.048 MHz
2 Mb/s (Unbalanced)	1.8 kHz	5 kHz	300 Hz	2.048 MHz
2 Mb/s (Unbalanced)	6.4 kHz	20 kHz	1 kHz	2.048 MHz
2 Mb/s (Unbalanced)	100 kHz	500 kHz	30 kHz	2.048 MHz
34 Mb/s	2.5 kHz	10 kHz	300 Hz	34.368 MHz
34 Mb/s	8 kHz	5 kHz	300 Hz	34.368 MHz
34 Mb/s	26 kHz	20 kHz	1 kHz	34.368 MHz
34 Mb/s	100 kHz	500 kHz	30 kHz	34.368 MHz
34 Mb/s	800 kHz	2 MHz	100 kHz	34.368 MHz
140 Mb/s	2.5 kHz	10 kHz	300 Hz	139.264 MHz
140 Mb/s	10 kHz	50 kHz	3 kHz	139.264 MHz
140 Mb/s	50 kHz	200 kHz	10 kHz	139.264 MHz
140 Mb/s	3.5 MHz	10 MHz	300 kHz	139.264 MHz
STM-0E	2.5 kHz	10 kHz	300 Hz	51.84 MHz
STM-0E	5 kHz	20 kHz	1 kHz	51.84 MHz
STM-0E	10 kHz	50 kHz	3 kHz	51.84 MHz
STM-0E	26 kHz	100 kHz	3 kHz	51.84 MHz
STM-0E	400 kHz	1 MHz	30 kHz	51.84 MHz
STM-1E	5 kHz	20 kHz	1 kHz	155.52 MHz
STM-1E	10 kHz	50 kHz	3 kHz	155.52 MHz
STM-1E	26 kHz	100 kHz	3 kHz	155.52 MHz
STM-1E	1.3 MHz	2 MHz	300 kHz	155.52 MHz
STM-4	10 kHz *(first test)*	50 kHz	3 kHz	622.08 MHz
STM-4	10 kHz *(second test)*	50 kHz	3 kHz	622.08 MHz
STM-4	68 kHz	200 kHz	10 kHz	622.08 MHz
STM-4	600 kHz	2 MHz	100 kHz	622.08 MHz

6. Set up the CTS with the following sequence using the values specified in Table 4–7:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	*as specified in column 1 of Table 4–7*
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	Off
		Jitter Output	Clock 0.8 V
		Jitter Clock Rate	*as specified in column 1 of Table 4–7*

7. Adjust the spectrum analyzer **center frequency** if necessary to center the unjittered signal spectrum.

8. Continue the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On
		Jitter Frequency	*as specified in column 2 of Table 4–7 **
		Jitter Amplitude	*as specified in column 3 of Table 4–7 **

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

***NOTE**. During some jitter tests, the front-panel LOS light will turn on. This is a normal condition and not an indication of a failure.*

9. On the spectrum analyzer, observe the measured amplitude at the center frequency (allow the amplitude to stabilize after several sweeps).

10. Increase the generated Jitter Amplitude by the increment listed in column 4 of Table 4–7 using the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Amplitude	*increase by amount specified in column 4 of Table 4–7*

11. Press **DONE** after each change in jitter amplitude.

12. Repeat steps 9 through 11 until the measured amplitude at the center frequency decreases through its minimum and starts to increase.

13. If the tabulated initial increment (column 4 of Table 4–7) is not 0.01UI, repeat steps 9 and 11 using a 0.01UI increment to find the minimum measured amplitude at the center frequency.

14. Verify that the Jitter Amplitude setting on the CTS, which corresponds to the minimum center-frequency amplitude, is between the limits listed in column 5 of Table 4–7.

Continue with step 15 on page 4–120.

Table 4–7: CTS Generation Setups

Transmit/Clock Rate	Jitter Frequency	Initial Jitter Amplitude	Initial Increment	Jitter Limits
2 Mb/s (Unbalanced)	2.5 kHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
2 Mb/s (Unbalanced)	1.8 kHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
2 Mb/s (Unbalanced)	6.4 kHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
2 Mb/s (Unbalanced)	100 kHz	0.68 UI	0.01 UI	0.70 to 0.83 UI
34 Mb/s	2.5 kHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
34 Mb/s	8 kHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
34 Mb/s	26 kHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
34 Mb/s	100 kHz	0.68 UI	0.01 UI	0.70 to 0.83 UI
34 Mb/s	800 kHz	0.68 UI	0.01 UI	0.70 to 0.83 UI
140 Mb/s	2.5 kHz	1.62 UI	0.02 UI	1.63 to 1.89 UI
140 Mb/s	10 kHz	8.2 UI	0.1 UI	8.27 to 9.23 UI
140 Mb/s	50 kHz	2.5 UI	0.05 UI	2.57 to 2.93 UI
140 Mb/s	3.5 MHz	0.68 UI	0.01 UI	0.69 to 0.84 UI
STM-0E	2.5 kHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
STM-0E	5 kHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
STM-0E	10 kHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
STM-0E	26 kHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
STM-0E	400 kHz	0.68 UI	0.01 UI	0.70 to 0.83 UI
STM-1E	5 kHz	1.62 UI	0.02 UI	1.63 to 1.89 UI
STM-1E	10 kHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
STM-1E	26 kHz	5.4 UI	0.1 UI	5.42 to 6.08 UI
STM-1E	1.3 MHz	0.68 UI	0.01 UI	0.69 to 0.84 UI
STM-4	10 kHz *(first test)*	1.55 UI	0.05 UI	1.56 to 1.96 UI
STM-4	10 kHz *(second test)*	8.2 UI	0.1 UI	8.20 to 9.30 UI
STM-4	68 kHz	5.3 UI	0.1 UI	5.35 to 6.15 UI
STM-4	600 kHz	0.6 UI	0.02 UI	0.62 to 0.91 UI

15. Set up the CTS with the following sequence using values specified in Table 4–8:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Output	Line
RECEIVE	JITTER & WANDER	Jitter Measurement Range	*as specified in column 3 of Table 4–8*
		Jitter Input Filter	*as specified in column 4 of Table 4–8*
RESULTS	MAIN RESULTS	*none*	Jitter/Wander

16. Press the **START/STOP** button, and verify that the START/STOP light is on.

17. Wait 30 seconds for the test to complete.

18. Verify that the current peak-to-peak jitter measurement by the CTS is between the limits in column 5 of Table 4–8.

19. Repeat steps 5 through 18 for each row in Tables 4–6, 4–7, and 4–8.

Table 4–8: CTS Measurement Setups

Transmit Rate	Jitter Frequency	Jitter Range	Jitter Filter	Measured Jitter Limits
2 Mb/s (Unbalanced)	2.5 kHz	Normal	Wideband	1.635 to 1.885 UI
2 Mb/s (Unbalanced)	1.8 kHz	Extended	Wideband	8.17 to 9.33 UI
2 Mb/s (Unbalanced)	6.4 kHz	Normal	Wideband	2.570 to 2.925 UI
2 Mb/s (Unbalanced)	100 kHz	*— (not tested)*	*— (not tested)*	*— (not tested)*
34 Mb/s	2.5 kHz	Normal	Wideband	1.630 to 1.885 UI
34 Mb/s	8 kHz	Extended	Wideband	8.27 to 9.23 UI
34 Mb/s	26 kHz	Normal	Wideband	2.570 to 2.925 UI
34 Mb/s	100 kHz	Normal	Wideband	0.685 to 0.845 UI
34 Mb/s	800 kHz	*— (not tested)*	*— (not tested)*	*— (not tested)*
140 Mb/s	2.5 kHz	Normal	Wideband	1.625 to 1.880 UI
140 Mb/s	10 kHz	Extended	Wideband	8.27 to 9.23 UI
140 Mb/s	50 kHz	Normal	Wideband	2.570 to 2.925 UI
140 Mb/s	3.5 MHz	*— (not tested)*	*— (not tested)*	*— (not tested)*
STM-0E	2.5 kHz	Normal	Wideband	1.630 to 1.885 UI
STM-0E	5 kHz	Normal	Wideband	1.630 to 1.890 UI
STM-0E	10 kHz	Extended	Wideband	8.270 to 9.230 UI
STM-0E	26 kHz	Normal	Wideband	2.570 to 2.925 UI
STM-0E	400 kHz	*— (not tested)*	*— (not tested)*	*— (not tested)*
STM-1E	5 kHz	Normal	Wideband	1.625 to 1.880 UI
STM-1E	10 kHz	Extended	Wideband	8.27 to 9.23 UI
STM-1E	26 kHz	Normal	Wideband	5.420 to 6.075 UI
STM-1E	1.3 MHz	*— (not tested)*	*— (not tested)*	*— (not tested)*
STM-4	10 kHz (first test)	Normal	Wideband	1.590 to 1.915 UI
STM-4	10 kHz (second test)	Extended	Wideband	8.19 to 9.22 UI
STM-4	68 kHz	Normal	Wideband	5.385 to 6.110 UI
STM-4	600 kHz	Normal	Highband	0.605 to 0.810 UI

Low-Amplitude Jitter Tests (CTS 750 Option 14 only)

Perform the following setup to prepare for the Low-Amplitude Jitter Tests.

Equipment Required	Spectrum analyzer (item 12) 75 Ω BNC coaxial cable (item 19), three required Optical fiber cable (item 13) 75 Ω to 50 Ω impedance converter (item 18) N-to-BNC adapter (item 27)
Prerequisites	All prerequisites listed on page 4–20 All previous Physical Layer Tests
Time Required	Approximately 60 minutes

1. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

2. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

CAUTION. *To prevent damage to the spectrum analyzer, follow the next step carefully before completing the instrument hookup.*

3. Perform the initial setup of the spectrum analyzer with the following steps:

   a. Set the reference level to **0 dBm**.

   b. Set the vertical scale factor to **10 dB/division**.

   c. Set the sweep to **free run**.

   d. Set the sweep to **auto** (or **coupled**).

4. Connect all CTS inputs and outputs in a loop-back configuration. Also, connect the rear-panel jitter clock output (J/CLK) to the spectrum analyzer RF input as shown in Figure 4–41.

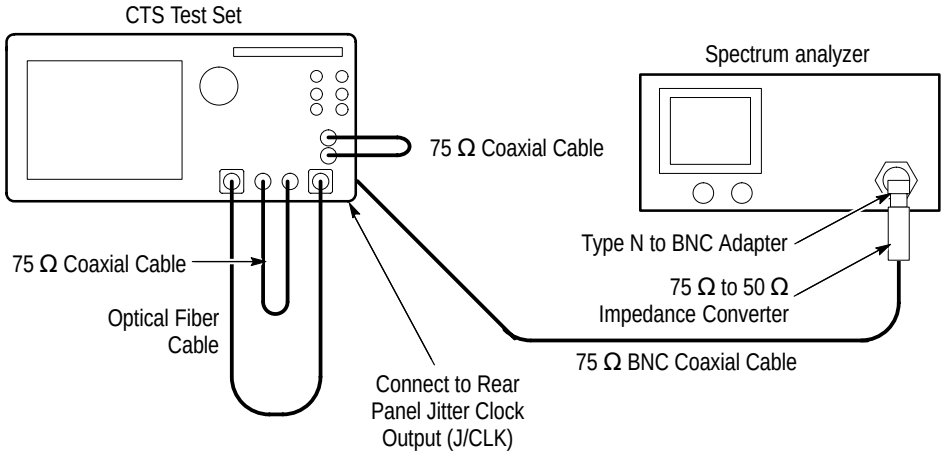

Figure 4–42: High Amplitude Jitter Test Hookup

***NOTE**. In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. The three tables that follow describe the specific conditions for each test. You will repeat the process for each row in the tables.*

5. For each row in Table 4–9, set up the spectrum analyzer as follows:

   a. Set the span (total over 10 divisions) to the value in column 3 of Table 4–9.

   b. Set both the resolution bandwidth and video bandwidth to the value in column 4 of Table 4–9.

   c. Set the center frequency to the value in column 5 of Table 4–9.

Table 4–9: Spectrum Analyzer Setups

Transmit Rate	Jitter Frequency	Ten-Division Span	Resolution Bandwidth and Video Bandwidth	Center Frequency
2 Mb/s (Unbalanced)	50 kHz	200 kHz	10 kHz	2.048 MHz
2 Mb/s (Unbalanced)	100 kHz	500 kHz	30 kHz	2.048 MHz
34 Mb/s	800 kHz	2 MHz	100 kHz	34.368 MHz
140 Mb/s	400 kHz	1 MHz	30 kHz	139.264 MHz
140 Mb/s	3.5 MHz	10 MHz	300 kHz	139.264 MHz
STM-0E	400 kHz	1 MHz	30 kHz	51.84 MHz
STM-1E	650 kHz	2 MHz	100 kHz	155.52 MHz
STM-1E	1.3 MHz	5 MHz	300 kHz	155.52 MHz
STM-4	3 MHz	200 kHz	10 kHz	622.08 MHz

6. Set up the CTS with the following sequence using the values specified in Table 4–10:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	*as specified in column 1 of Table 4–10*
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	Off
		Jitter Output	Clock 0.8 V
		Jitter Clock Rate	*as specified in column 1 of Table 4–10*
		Jitter Frequency	*as specified in column 2 of Table 4–10 **
		Jitter Amplitude	*as specified in column 3 of Table 4–10 **

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

7. Adjust the spectrum analyzer **center frequency** if necessary to center the unjittered signal spectrum.

8. Set the spectrum analyzer vertical scale factor to **2 dB/division**.

9. Adjust the spectrum analyzer reference level to set the peak at the center frequency to the top graticule line.

10. Continue the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On

11. On the spectrum analyzer display, measure the amplitudes (in dBm) of the center frequency (CF), the first side lobe above the carrier (USL), and the first side lobe below the carrier (LSL).

12. Perform the following calculations on the measured amplitudes:

$$Side\ band\ level\ (dB) = Amplitude_{USL} + Amplitude_{LSL} - (2 \times Amplitude_{CF})$$

$$Jitter\ (UI) = (Side\ band\ level \times 0.01354) + 0.4541$$

13. Verify that the calculated jitter from step 12 is between the limits listed in column 3 of Table 4–10.

Table 4–10: CTS Generation Setups

Transmit Rate	Jitter Frequency	Jitter Amplitude	Calculated Jitter Limits
2 Mb/s	50 kHz	0.3 UI	0.266 to 0.356 UI
2 Mb/s	100 kHz	0.3 UI	0.266 to 0.356 UI
34 Mb/s	800 kHz	0.5 UI	0.447 to 0.557 UI
140 Mb/s	400 kHz	0.5 UI	0.437 to 0.567 UI
140 Mb/s	3.5 MHz	0.5 UI	0.437 to 0.567 UI
STM-0E	400 kHz	0.5 UI	0.447 to 0.557 UI
STM-1E	650 kHz	0.5 UI	0.437 to 0.567 UI
STM-1E	1.3 MHz	0.5 UI	0.437 to 0.567 UI
STM-4	3 MHz	0.3 UI	0.186 to 0.436 UI

Continue with step 14 on page 4–127.

14. Set up the CTS with the following sequence using values specified in Table 4–11:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Output	Line
RECEIVE	JITTER & WANDER	Jitter Measurement Range	*as specified in column 3 of Table 4–11*
		Jitter Input Filter	*as specified in column 4 of Table 4–11*
RESULTS	MAIN RESULTS	*none*	Jitter/Wander

15. Press the **START/STOP** button, and verify that the START/STOP light is on.

16. Wait 30 seconds for the test to complete.

17. Calculate the minimum and maximum jitter limits. To do this, start with the calculated jitter result from step 12, and then add or subtract the amounts shown in columns 5 and 6 of Table 4–11.

18. Verify that the current peak-to-peak jitter measurement by the CTS is within the jitter limits calculated in step 17.

19. Repeat steps 5 through 18 for each row in Tables 4–9, 4–10, and 4–11.

Table 4–11: CTS Measurement Setups

Transmit Rate	Jitter Frequency	Jitter Range	Jitter Filter	Minimum Jitter Limit *	Maximum Jitter Limit *
2 Mb/s (Unbalanced)	50 kHz	Normal	Wideband	J – 0.061 UI	J + 0.049 UI
2 Mb/s (Unbalanced)	100 kHz	Normal	Highband – High Q	J – 0.151 UI	J – 0.029 UI
34 Mb/s	800 kHz	Normal	Highband	J – 0.207 UI	J – 0.077 UI
140 Mb/s	400 kHz	Normal	Wideband	J – 0.062 UI	J + 0.068 UI
140 Mb/s	3.5 MHz	Normal	Highband	J – 0.207 UI	J – 0.077 UI
STM-0E	400 kHz	Normal	Highband	J – 0.207 UI	J – 0.077 UI
STM-1E	650 kHz	Normal	Highband	J – 0.067 UI	J + 0.063 UI
STM-1E	1.3 MHz	Normal	Wideband	J – 0.207 UI	J – 0.077 UI
STM-4	3 MHz	Normal	Wideband	J – 0.101 UI	J + 0.079 UI

*** The variable "J" refers to the calculateded jitter result from step 12.**

You have completed the CTS performance verification procedures.

Adjustment Procedures

This section contains information needed to adjust the CTS. There are only three types of adjustments you can perform on the CTS. Table 5–1 lists the adjustments and when they are required.

Table 5–1: When to Adjust the CTS

Adjustment	Routine Adjustment	Adjustment After Repair
Setting the CTS serial number	Not required	After replacing the CPU board
Adjusting the internal clock frequency	Only if the clock frequency is out of tolerance	After replacing the Clock board or Low-Voltage Power Supply
Adjusting the display monitor	Not required	After replacing the monitor or the Low-Voltage Power Supply
Calibrating jitter generation and measurement (Option 14 only)	Before taking critical measurements	After replacing JAWA/JAWG assembly, Tributary assembly, or Plug-in Interface Module.

Equipment Required

The tools and test equipment needed to adjust the CTS are listed in Table 5–2 on page 5–2. Setting the serial number or adjusting the internal clock frequency requires communication with the CTS through its GPIB or RS-232 port. There are several ways to set up bus communication:

- Connect a terminal or a PC with a terminal-emulator program to the CTS RS-232 port.
- Connect a GPIB controller with talker/listener software to the CTS GPIB port.
- If you have a Tektronix VX4610 and a PC controller, you can use the UI4610 Software, a standard accessory of the VX4610, to communicate with your CTS. The UI4610 Software contains a GPIB talker/listener tool.

Table 5–2: Required Tools and Equipment for Adjustment

Item Number and Description		Minimum Requirements	Example	Purpose
1	Universal Counter/Timer	60 MHz frequency measurement capability; 0.25 ppm time base accuracy; 9 digits; averaging to 10^8	Tektronix DC 5010 Digital Counter/Timer with TM 5000 mainframe	Adjusting the internal clock frequency
2	50 Ω SMB-to-BNC Coaxial Cable	50 Ω impedance; SMB female connector on one end, BNC male connector on the other	Tektronix P6041	Adjusting the internal clock frequency
3	External Graticule Test Fixture	Tektronix part number 067-0206-01	Tektronix part number 067-0206-01	Adjusting display monitor size and position
4	Photometer	0.1 to 200 fL	Tektronix J17 LumaColor Photometer with J1803 Luminance Head	Adjusting display monitor brightness and contrast
5	Terminal, Terminal Emulator, or Controller	RS-232 or GPIB talker/listener capability	PC controller with Tektronix UI4610 software (standard accessory to VX4610)	Setting the serial number Adjusting the internal clock frequency
6	Adjustment Tool	0.075 inch slotted screwdriver	Tektronix part number 003-1433-01 (standard probe adjustment tool)	Adjusting the internal clock frequency Adjusting the display monitor
7	Flat-Bladed Screwdriver	General purpose, 0.25 inch, slotted screwdriver	Xcelite R-144	Adjusting the internal clock frequency

Procedures

The following adjustment procedures are independent of one another and may be performed in any order. Allow the CTS a 20-minute warm-up period before performing any adjustments.

Setting the Serial Number

Use this procedure to set the CTS serial number after you have replaced the CPU board.

Equipment Required	Terminal, Terminal Emulator, or Controller (item 5)
Time Required	Approximately five minutes

1. Connect the terminal, terminal emulator, or controller to the RS-232 or GPIB port on the rear panel of the CTS. Set the communication port parameters as

needed to establish communication. The CTS communication port settings are accessible with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	REMOTE CONTROL	*as needed*	*as needed*

2. Using the terminal or controller, send the following command (substitute the actual serial number for the parameter <s/n>):

```
SYSTem:SERIal "<s/n>";
```

For example, to set the serial number to B010100, send the command `SYSTem:SERIal "B010100";`.

3. Display the serial number with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	INSTR CONFIG	*none*	*none*

4. Verify that the displayed serial number is correct. If so, you have completed this procedure. If it is not correct, reverify the communication between the terminal or controller and the CTS and repeat the procedure.

Adjusting the Internal Clock Frequency

You should adjust the internal clock frequency only if you have replaced the Clock board, replaced the Low-Voltage Power Supply, or if the internal clock frequency is out of tolerance. You should perform this adjustment if the CTS fails the physical layer test *Checking Internal Clock Accuracy*, which begins on page 4–46.

Equipment Required	Universal Counter/Timer (item 1) SMB-to-BNC Coaxial Cable (item 2) Terminal, Terminal Emulator, or Controller (item 5) Adjustment Tool (item 6) Flat-Bladed Screwdriver (item 7)
Time Required	Approximately one hour

1. Connect the terminal, terminal emulator, or controller to the RS-232 or GPIB port on the rear panel of the CTS. Set the communication port parameters as needed to establish communication. The CTS communication port settings are accessible with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	REMOTE CONTROL	*as needed*	*as needed*

2. Connect the SMB-to-BNC coaxial cable from the CAL output on the CTS rear panel to the Universal Counter/Timer as shown in Figure 5–1.

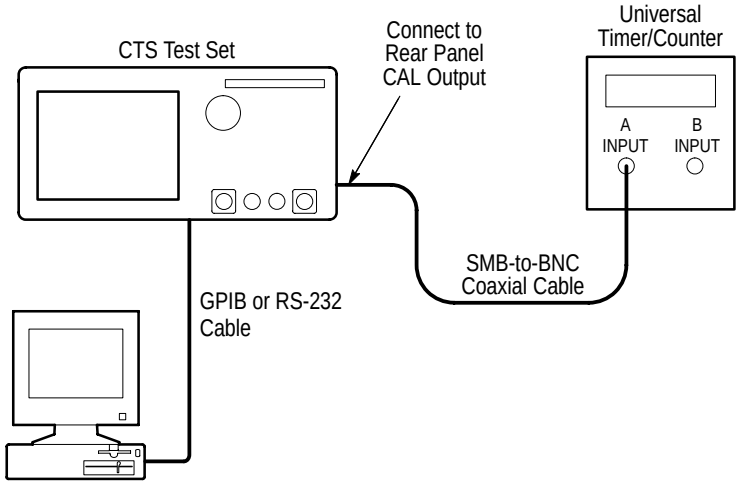

Figure 5–1: Internal Clock Frequency Adjustment Connections

3. Using the terminal or controller, send the following command:

```
DIAGnostic:CALIbrate:CLOCk 0.0;
```

4. To measure the internal clock frequency, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup

5. Set the Universal Counter/Timer as follows:

   a. Set input impedance to **50 Ω**.

b. Set input coupling to **AC**.

c. Set number of averages to $\mathbf{10^8}$.

d. Set measurement mode to **Frequency**.

6. Verify that the Universal Counter/Timer reads between 51,839,960 Hz and 51,840,238 Hz (inclusive). If it does, the internal clock frequency is within tolerance and you have completed this procedure. Proceed to step 7 only if the internal clock frequency is out of tolerance.

7. Turn off power to the CTS, disconnect it from the test setup, and unplug the power cord from the AC source.

8. To adjust the CTS internal clock frequency, you must remove the line cord, rear cover, and cabinet. Refer to the information beginning on page 6–26 for the procedures to remove these parts.

WARNING. *High voltages are accessible on the power supply and the monitor assembly. Do not touch these circuit boards when the power is on.*

9. After the cabinet has been removed, reconnect the CTS to the setup shown in Figure 5–1, reconnect the line cord, apply power, and allow the CTS to warm up again for at least 20 minutes.

10. When the warm-up is complete, locate the crystal oscillator on the right side of the CTS (see Figure 5–2).

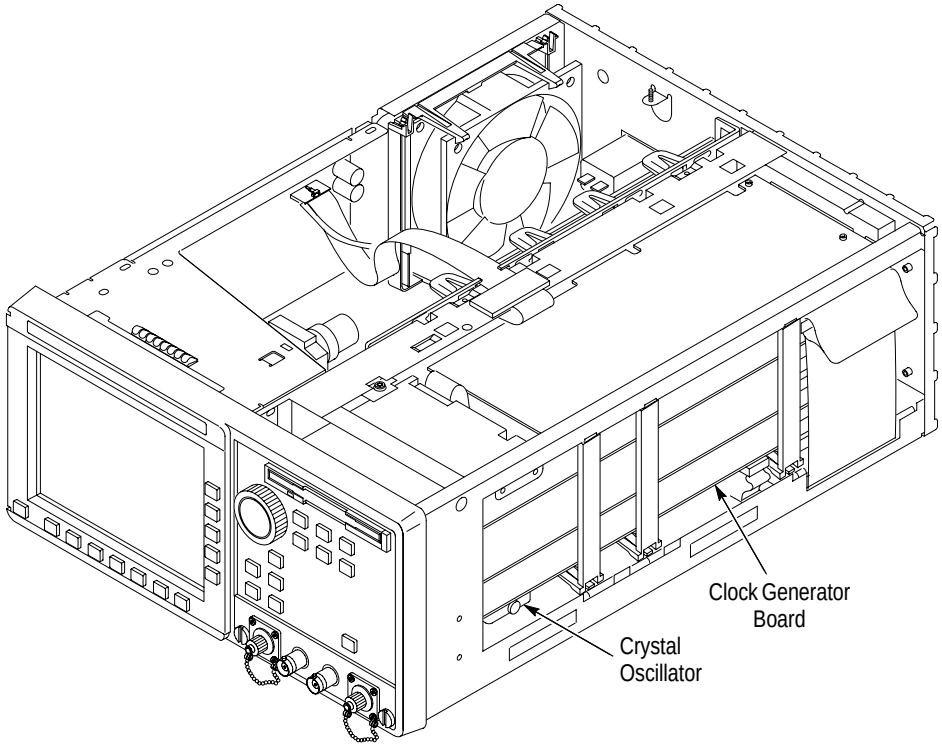

Figure 5–2: Location of Crystal Oscillator

11. Using the flat-bladed screwdriver, carefully remove the slotted screw on the side of the crystal oscillator to access the adjustment screw.

12. Insert the adjustment tool into the crystal and adjust the internal clock frequency to 51,840,000 Hz ± 10 Hz.

13. Replace the slotted screw that covers the crystal oscillator adjustment screw.

14. Using the terminal or controller, send the following command to set the clock calibration date, where `yy,mm,dd` is the current year, month, and day:

```
DIAGnostic:CALIbrate:CDAT yy,mm,dd;
```

15. The internal clock adjustment is complete. Turn off power and reassemble the CTS according to the procedure beginning with step 9 on page 6–29.

Adjusting the Display Monitor

You should perform these adjustments only if you have replaced the monitor, replaced the Low-Voltage Power Supply, or if the display quality is unsatisfactory.

Equipment Required	External Graticule Test Fixture (item 3) Photometer (item 4) Adjustment Tool (item 6) Flat-Bladed Screwdriver (item 7)
Time Required	Approximately one hour

1. To adjust the display monitor, you must remove the line cord, rear cover, and cabinet. Refer to the information beginning on page 6–26 for the procedures to remove these parts.

WARNING. *High voltages are accessible on the power supply and the monitor assembly. Do not touch these circuit boards when the power is on. Do not touch the CRT anode button even if the power is off. Wear safety glasses when working with the CRT.*

2. After the cabinet has been removed, reconnect the CTS to the setup shown in Figure 5–1, reconnect the line cord, apply power, and allow the CTS to warm up for at least 20 minutes.
3. To prepare the J17 LumaColor Photometer to make measurements, perform the following steps:
   a. With the photometer power turned off, connect the J1803 Luminance Head to the photometer.
   b. Turn the photometer power on. The photometer performs a brief self test.
   c. Press the **ALT DISP** button once and the **UNITS** button once.
   d. Verify that the photometer displays the letters WHT in the upper-left corner, the letters fL in the upper-right corner, and a four-digit number in the center. If the display does not contain this information, turn off the power and repeat steps b through d.
4. Locate the monitor adjustments along the top-left side of the CTS (see Figure 5–3).

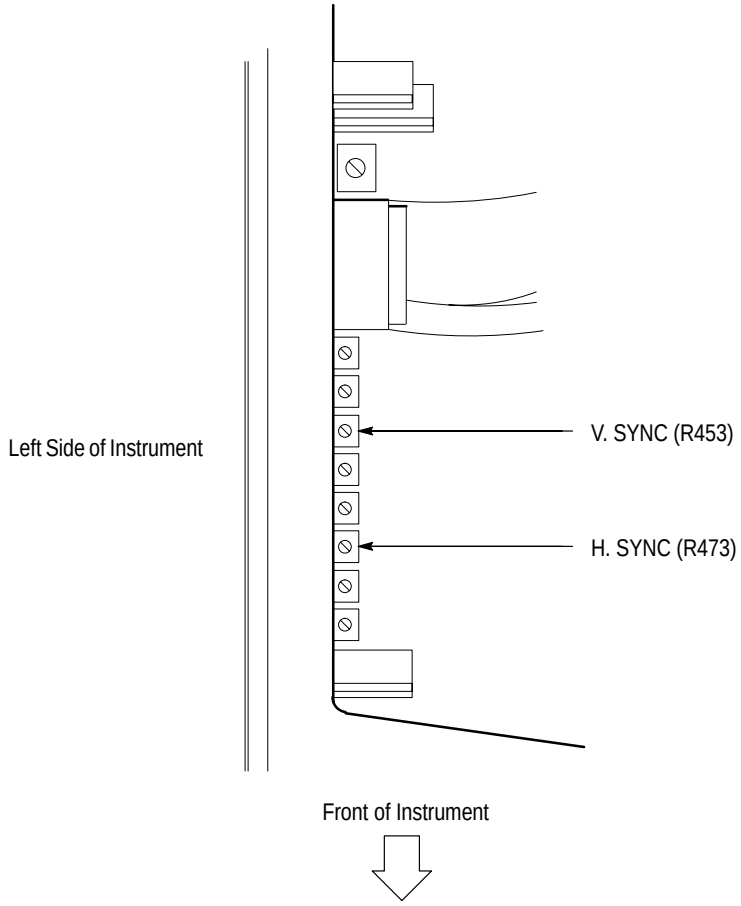

Figure 5–3: Monitor Adjustment Locations

5. To adjust the vertical and horizontal sync, perform the following steps:

   a. If the display rolls vertically, adjust **V. SYNC (R453)** to the center of the stable display range.

   b. If diagonal lines are present on the display, adjust **H. SYNC (R473)** to the center of the stable display range.

6. To adjust the display brightness, perform the following steps:

a. Set the CTS to display a gray field pattern (see Figure 5–4) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Gray Field
		Self Test Control	RUN

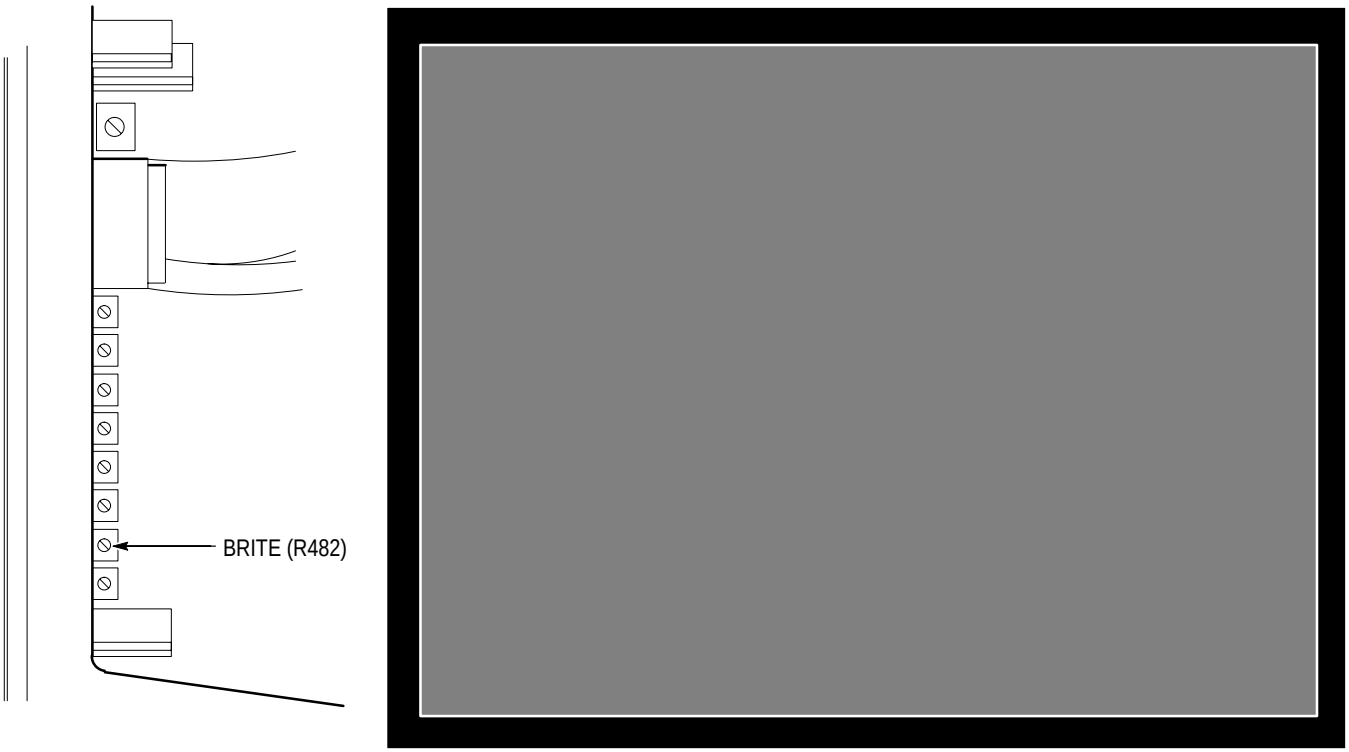

Figure 5–4: Brightness Adjustment and Gray Field Pattern

b. Hold the J1803 Luminance Probe against the faceplate of the monitor at the center of the screen.

c. Verify that the display brightness is within the tolerance from 1.4 fL to 2.1 fL (inclusive).

d. If the display brightness is out of tolerance, adjust **BRITE (R482)** for a reading of approximately 1.75 fL.

7. To adjust video gain perform the following steps:

a. Set the CTS to display a white box pattern (see Figure 5–5) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	White Box
		Self Test Control	RUN

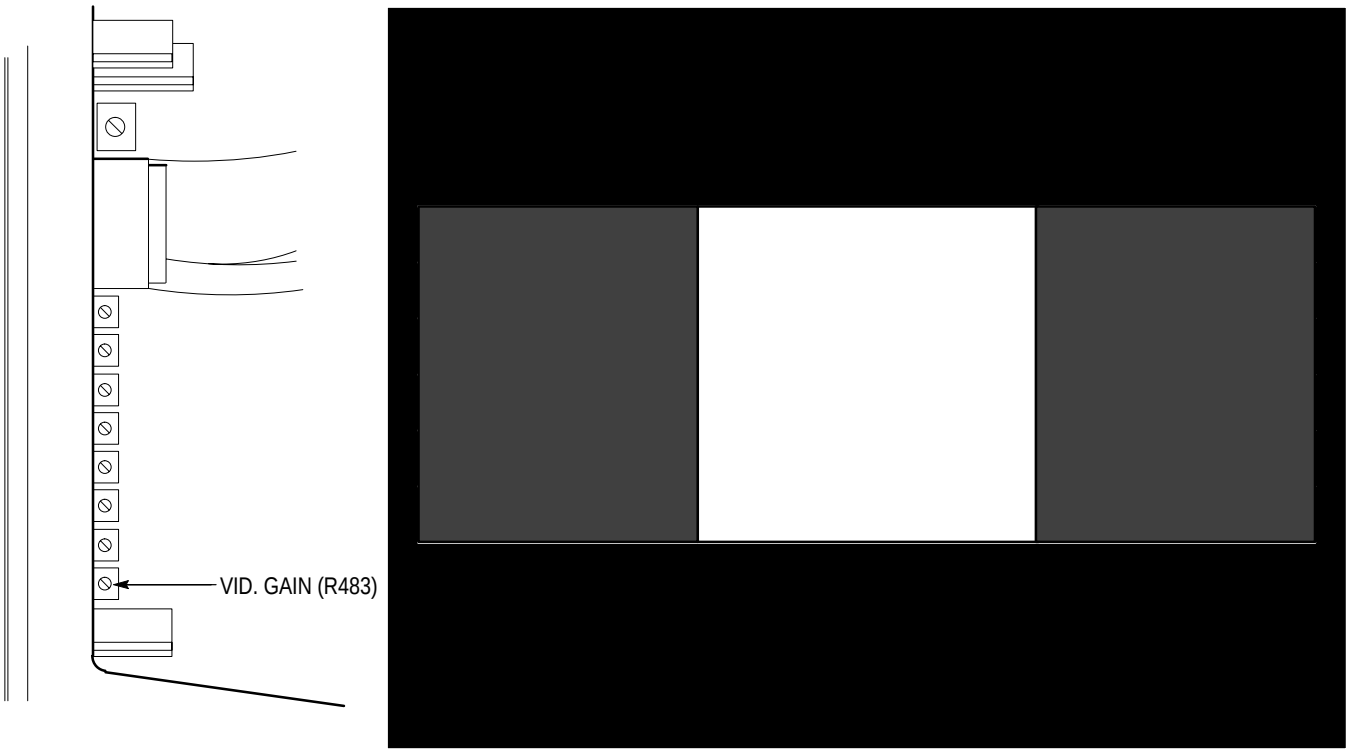

Figure 5–5: Video Gain Adjustment and White Box Pattern

b. Hold the J1803 Luminance Probe against the faceplate of the monitor at the center of the screen.

c. Verify that the display brightness is within the tolerance from 35 fL to 53 fL (inclusive).

d. If the display brightness is out of tolerance, adjust **VID. GAIN (R483)** for a reading of approximately 44 fL.

e. If you adjusted the video gain, repeat steps 6 and 7 until both the brightness and video gain measurements are within tolerance.

8. To adjust the display focus, perform the following steps:

a. Set the CTS to display a composite test pattern (see Figure 5–6) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Composite
		Self Test Control	RUN

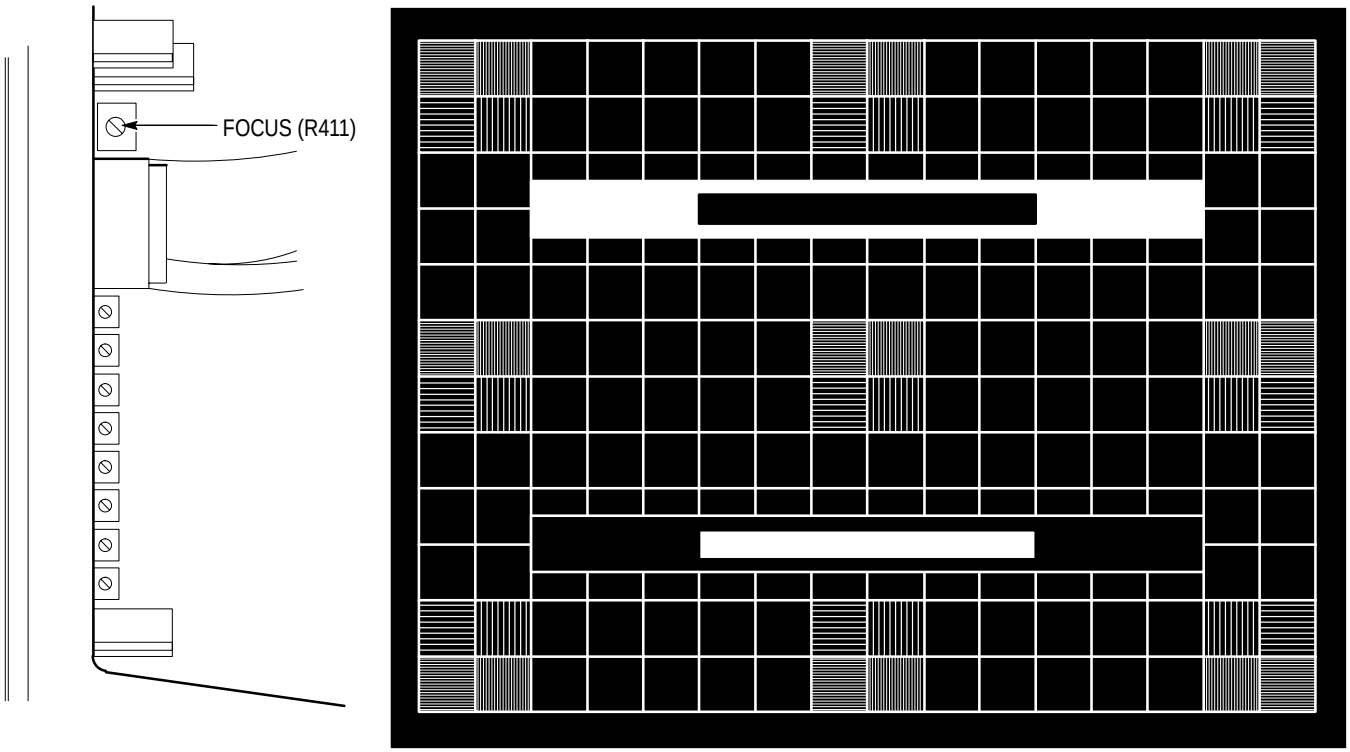

Figure 5–6: Focus Adjustment and Composite Test Pattern

b. Adjust **FOCUS (R411)** for best overall focus at all four corners and at the center of the screen.

c. Press any CTS front-panel button to continue.

9. To adjust the display position and size, perform the following steps:

a. Set the CTS to display a test grid pattern (see Figure 5–7) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Test Grid
		Self Test Control	RUN

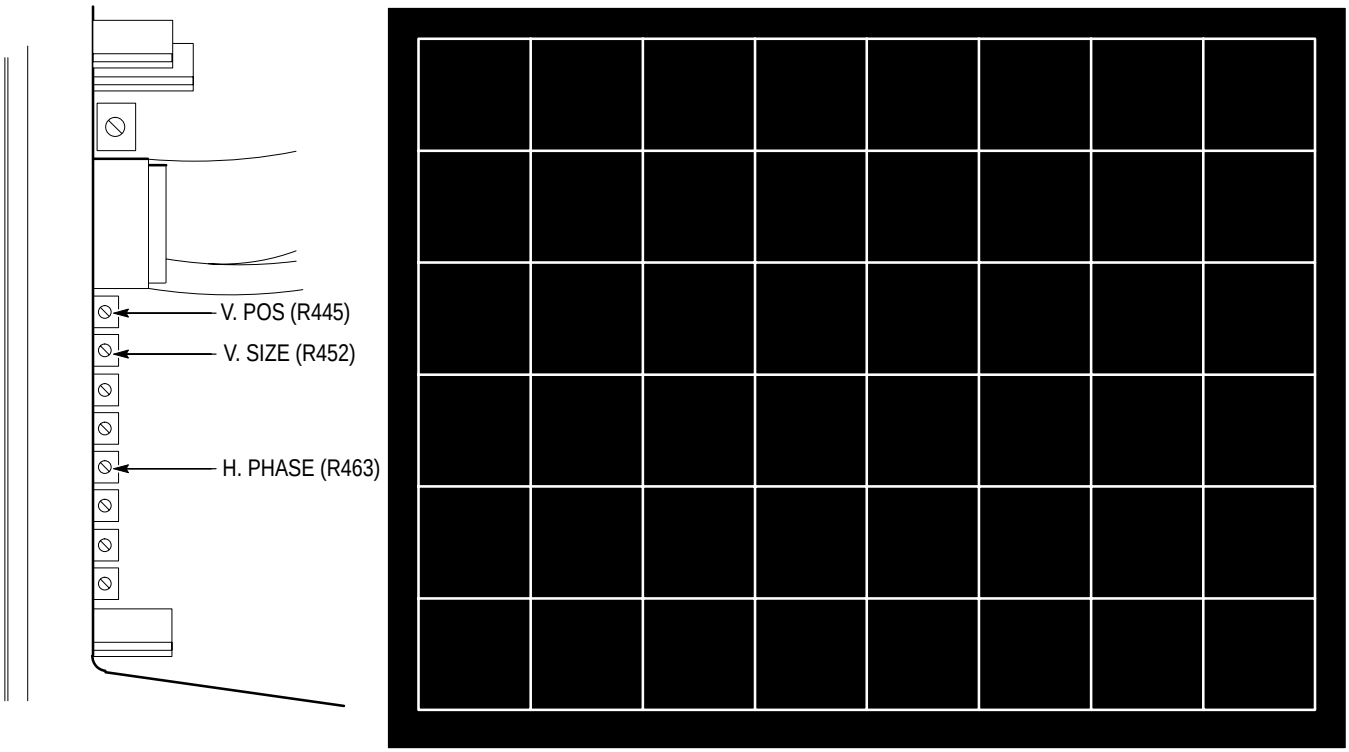

Figure 5–7: Position and Size Adjustments and Test Grid Pattern

b. To make the following adjustments, use the External Graticule Test Fixture as a visual reference (see Figure 5–8). You can position the test fixture in the CTS bezel opening as necessary to align it to the displayed test pattern. Start by positioning the External Graticule Test Fixture so that it is centered (approximately) in the bezel opening.

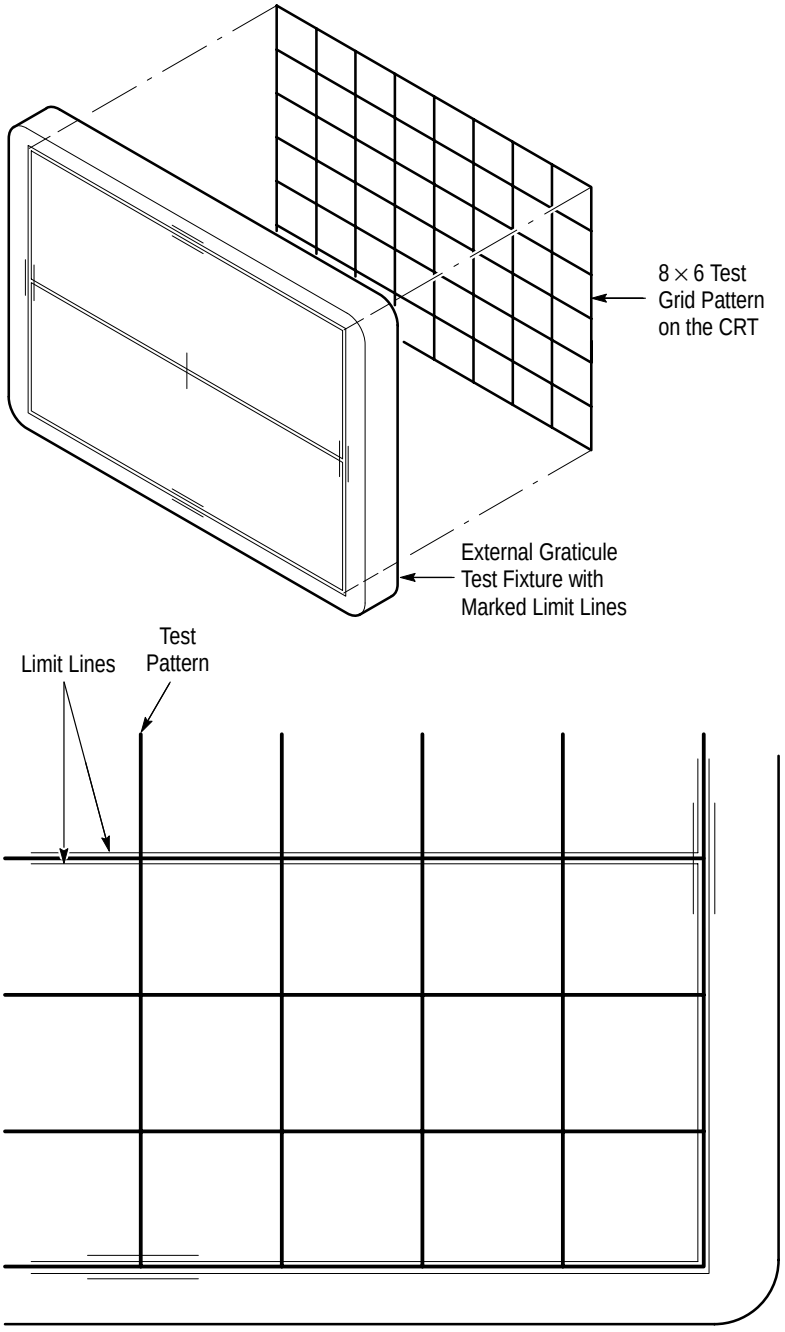

Figure 5–8: External Graticule Limit Lines

c. Adjust **V. POS (R445)** so that the horizontal centerline is within the limit lines of the External Graticule Test Fixture. (See Figure 5–8.) You may need to rotate the External Graticule Test Fixture slightly to see the horizontal centerline within its limits across the entire display.

d. Adjust **V. SIZE (R452)** so that the top and bottom lines are within their limits. You can reposition the External Graticule Test Fixture as necessary to make this adjustment.

e. Reposition the External Graticule Test Fixture so that it is centered (approximately) in the CTS bezel opening.

f. Adjust **H. PHASE (R463)** so that the left and right lines are within their limits. You may need to rotate the External Graticule Test Fixture slightly to see the left and right lines within their limits across the entire display. If you cannot set both lines within their limits, adjust for best compromise.

10. The display monitor adjustment is complete. Turn off power and reassemble the CTS according to the procedure beginning with step 9 on page 6–29.

Calibrating Jitter Generation and Measurement

For Option 14 equipped test sets only, periodic calibration of the jitter generation and measurement systems is recommended to maintain best accuracy. You can execute built-in calibration routines before making critical measurements.

Equipment Required	None
Time Required	Approximately 90 minutes

To calibrate the jitter generation system:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	CALIBRATION	Calibration System	Jitter Generation
		Calibration Routine	All
		Calibration Control	Run

To calibrate the jitter measurement system:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	CALIBRATION	Calibration System	Jitter Measurement
		Calibration Routine	All
		Calibration Control	Run

A status message indicates that the calibration is running, has completed and has passed, or has failed. Select **Abort** to stop a calibration in progress.

Maintenance

This section contains the information needed to do periodic and corrective maintenance on the CTS 700-Series Test Sets. The following sections are included:

- Preparation — General information on preventing damage to internal modules when doing maintenance.
- Inspection and Cleaning — Information and procedures for inspecting the CTS and cleaning its external and internal modules.
- Removal and Replacement — Instructions for the removal of defective modules and replacement with new or repaired modules. Also included are instructions for disassembly of the CTS for cleaning.
- Troubleshooting — Information for isolating and troubleshooting failed modules. Included are troubleshooting trees and instructions for operating the CTS internal diagnostic routines.
- After-Repair Adjustments — List of which adjustment procedures you must perform after a module is replaced.
- Repackaging Instructions — Instructions on how to package the CTS for shipment.

Preparation

Procedures in this manual are for qualified service personnel only. Before performing any service procedures, read the safety summaries at the front of this manual. Read *Operating Information* before servicing the CTS.

Related Maintenance Procedures

Refer to these other sections for additional information and procedures related to doing maintenance:

- *Operating Information* contains instructions that you may find useful during service procedures.
- *Theory of Operation* contains a circuit description at the module level.
- *Performance Verification* can help isolate faulty modules by testing CTS performance.
- *Adjustment Procedures* addresses after-repair adjustments to the CTS. It contains a procedure for adjusting the CTS internal circuits.

- *Diagrams* contains a block diagram using individual modules as blocks and an interconnect diagram showing connections between the modules.
- *Mechanical Parts List* contains a list of field replaceable modules by part number.

Preventing ESD

When performing any service which requires internal access to the CTS, follow these precautions to prevent electrostatic discharge (ESD) damage to internal modules and their components:

CAUTION. *Static discharge can damage any semiconductor component in this CTS 700-Series Test Set.*

1. Minimize handling of static-sensitive modules.
2. Transport and store static-sensitive modules in their static-protected containers. Label any package that contains static-sensitive modules.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these modules. Perform service of static-sensitive modules only at a static-free work station.
4. Do not remove the CTS cabinet unless you have met precaution number 3, above. Consider all internal modules static-sensitive.
5. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
6. Handle circuit boards by their edges when possible.
7. Do not slide the modules over any surface.
8. Avoid handling modules in areas that have a floor or work-surface covering capable of generating a static charge.
9. Do not use high-velocity compressed air when cleaning dust from modules.

Inspection and Cleaning

Inspection and Cleaning describes how to inspect for dirt and damage and how to clean the exterior and interior of the CTS. You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent CTS malfunction and enhance its reliability.

How often to do maintenance depends on the severity of the environment in which you use the CTS. A proper time to perform preventive maintenance is just before CTS adjustment.

General Care

The cabinet helps keep dust out of the CTS and is a major component of its cooling system. It should normally be in place when operating the CTS. The optional CTS front cover protects the front panel and display from dust and damage. Install the front cover when storing or transporting the CTS.

Inspection and Cleaning Procedures

Inspect and clean the CTS as often as operating conditions require. The collection of dirt on components inside can cause them to overheat and break down. (Dirt acts as an insulating blanket, preventing efficient heat dissipation.) Dirt also provides an electrical conduction path that could cause a CTS failure, especially under high-humidity conditions.

CAUTION. *Avoid the use of chemical cleaning agents that might damage the plastics used in this CTS. Use only deionized water when cleaning the menu buttons or front-panel buttons. Use a 75% isopropyl alcohol solution as a cleaner and rinse with deionized water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.*

Avoid the use of high pressure compressed air when cleaning dust from the interior of the CTS. (High pressure air can cause electrostatic discharge.) Instead, use low pressure compressed air (about 9 psi).

Inspection — Exterior

Inspect the outside of the CTS for damage, wear, and missing parts using Table 6–1 as a guide. You should thoroughly check a CTS that appears to have been dropped or otherwise abused to verify correct operation and performance. Immediately repair defects that could cause personal injury or lead to further damage to the CTS.

Table 6–1: External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, front panel, and cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Replace defective module.
Front-panel knobs	Missing, damaged, or loose knobs.	Repair or replace missing or defective knobs.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective modules. Clear or wash out dirt.
Carrying handle and cabinet feet	Correct operation.	Replace defective module.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective modules.

Cleaning Procedure — Exterior

Clean the exterior of the CTS as follows:

WARNING. *To avoid injury or death, unplug the power cord from line voltage before cleaning the CTS. To avoid getting moisture inside the CTS during external cleaning, use only enough liquid to dampen the cloth or applicator.*

1. Remove loose dust on the outside of the CTS with a lint-free cloth.
2. Remove remaining dirt with a lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.
3. Clean the monitor screen with a lint-free cloth dampened with either isopropyl alcohol or, preferably, a gentle, general purpose detergent-and-water solution.

Cleaning Procedure — Optical Ports

If the CTS performance appears degraded, the optical fiber and optical port may be dirty. Clean the fiber connector with a clean cloth.

To clean an optical port:

1. Verify that the CTS has been turned off with the principal power switch on the rear panel.
2. Remove the four screws that attach the bulkhead connector to the front panel (see Figure 6–1).

3. Gently pull the bulkhead out of the unit and unscrew the fiber connector. Be careful not to pull beyond the fiber slack.

4. Using a soft, lint-free cloth with a high-quality glass cleaner, clean the tip of the fiber cable.

5. If available, use low-pressure compressed air or canned air to blow any dirt out of the bulkhead connector. If compressed air is not available, then the bulkhead will have to be taken apart and cleaned. Refer to the removal and replacement procedure *Optical Port Connector,* on page 6–22, for information about bulkhead disassembly.

6. After cleaning the bulkhead, reconnect the fiber and install the bulkhead. Be sure to reinstall the dustcap chain.

NOTE*. To keep cleaning to a minimum, install the dustcap when the optical port does not have a fiber attached.*

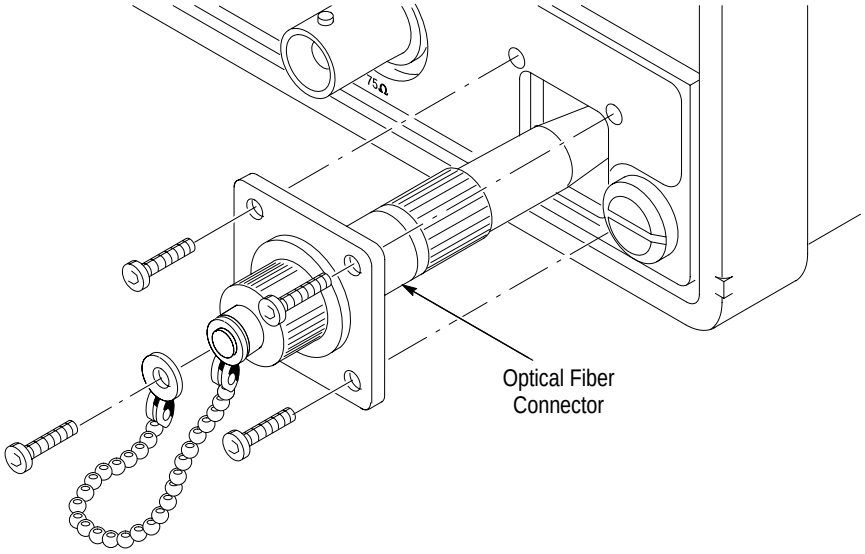

Figure 6–1: Removing the Optical Bulkhead Connector

Inspection — Interior

To access the inside of the CTS for inspection and cleaning, refer to *Removal and Replacement*, starting on page 6–9 in this section.

Inspect the internal portions of the CTS for damage and wear, using Table 6–2 as a guide. You should repair defects immediately.

If you replace any electrical module, perform the adjustment procedures beginning on page 5–1.

CAUTION. *To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the CTS.*

Table 6–2: Internal Inspection Check List

Item	Inspect For	Repair Action
Circuit boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Replace the failed module.
Solder connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Wiring and cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace modules with defective wires or cables.
Chassis	Dents and deformations	Straighten, repair, or replace chassis.

Cleaning Procedure — Interior

The interior cleaning procedure is as follows:

1. Blow off dust with dry, low-pressure, deionized air (approximately 9 psi).
2. Remove any remaining dust with a lint-free cloth dampened in isopropyl alcohol (75% solution) and rinse with warm deionized water. (A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards.)

NOTE*. If, after doing steps 1 and 2, a module is clean upon inspection, skip steps 3 through 7.*

If steps 1 and 2 do not remove all the dust or dirt, the CTS may be spray washed using a solution of 75% isopropyl alcohol by doing steps 3 through 7.

3. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see *Removal and Replacement* on page 6–9).

4. Spray wash dirty parts with the isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate.
5. Use hot (120° F to 140° F, 49° C to 60° C) deionized water to thoroughly rinse the parts.
6. Dry all parts with low-pressure, deionized air.
7. Dry all components and assemblies in an oven or drying compartment using low-temperature (125° F to 150° F, 52° C to 66° C) circulating air.

Lubrication

There is no periodic lubrication required.

Removal and Replacement

This section contains the following information:

- Preparatory information
- A list of equipment required to remove and disassemble all modules
- Module locator diagrams for finding the modules in the CTS
- Procedures for removal and replacement of the modules

Preparation

WARNING. *Before doing this or any other procedure in this manual, read the safety summaries found at the beginning of this manual. Also, to prevent possible injury to personnel or damage to the CTS 700-Series Test Set components, read* Supplying Operating Power *on page 2–1, and* Preventing ESD *on page 6–2.*

- Module disassembly procedures.

Before doing any procedure in this section, disconnect the power cord from the line voltage source. Failure to do so could cause serious injury or death.

Read these general instructions before removing a module:

1. Read the *Summary of Procedures* on page 6–10 to understand how the procedures are grouped. Then read *Equipment Required* on page 6–10 for a list of the tools needed to remove and install modules in the CTS.
2. Study Figure 6–2, which defines the sides of the CTS referred to by the procedures.
3. If you are removing a module for service, begin by doing the *Access Procedure* (page 6–11). By following the instructions in that procedure, you remove the module to be serviced while removing the minimum number of additional modules. Reverse the *Access Procedure* to reassemble the CTS after you have serviced and reinstalled a module.
4. If you are disassembling the CTS for cleaning, go to the *Disassembly for Cleaning* procedure on page 6–65.

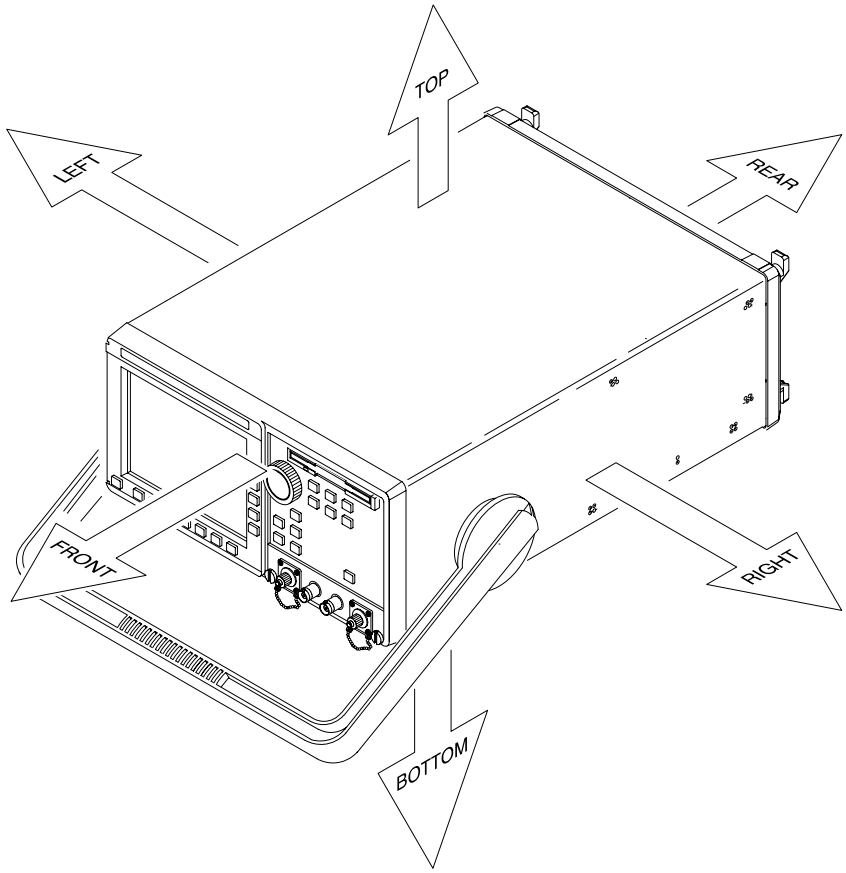

Figure 6–2: CTS 700-Series Test Set Orientation

Summary of Procedures

The procedures are described in the order in which they appear in this section. These procedures are also listed in the *Table of Contents*.

- The *Access Procedure* on page 6–11 first directs you to the procedures that remove any modules that must be removed to access the module to be serviced. It then directs you to the procedure to remove that module.
- *Procedures for Module Removal and Installation* on page 6–22 are the procedures for removing modules. These procedures assume you have done the access procedure.
- *Disassembly for Cleaning* on page 6–65 is a procedure, based on the module removal procedures just described, that removes all modules for cleaning. Instructions for cleaning are found in *Inspection and Cleaning*, on page 6–3. The *Disassembly for Cleaning* procedure does not use the access procedure.

Equipment Required

The following tools are required to completely disassemble the CTS into its modules. The tools required to remove an individual module are listed in the first

step of its procedure. All the tools are standard tools readily available from tool suppliers.

Table 6–3: Tools Required for Module Removal

Item No.	Name	Description
1	Screwdriver handle	Accepts Torx-driver bits.
2	T-15 Torx tip	Torx-driver bit for T-15 size screw heads.
3	T-20 Torx tip	Torx-driver bit for T-20 size screw heads. Used only for removal of the cabinet handle.
4	Flat-bladed screwdriver	Screwdriver for removing standard-head screws.
5	Needle-nose pliers	Standard tool. Used for removing EMI gaskets.
6	Duck-bill pliers	4 inch. Used for removing the Low-Voltage Power Supply.
7	Pozidriv screwdriver	Used for removing disk drive.
8	Nut driver, 5/16 inch	Used for removing earth ground cables.
9	Nut driver, 3/16 inch	Used for removing GPIB connector shell and EMI gasket.
10	Nut driver, 1/4 inch	Used for removing A09 Main Protocol assembly.
11	Nut driver, 9/32 inch	Used for removing EMI gasket.
12	Hex key screwdriver, 1/16 inch	Used for knob removal.
13	Flat-bladed spudger	A probe-like tool, made of wood or fiber, with a tip like a flat bladed screwdriver. Used to press EMI gaskets into place.
14	Slip-jaw pliers	Used for removing the front feet from the cabinet.
15	Soldering iron	15 W. Used for removal of some cables.
16	CTS 700-Series Test Set Front Cover	This cover protects the front of the CTS 700-Series Test Set when positioned face down in the removal procedures.

Access Procedure

Begin with this procedure when you have identified a module to be removed for service and have read *Preparation* and *Summary of Procedures* on pages 6–9 and 6–10.

1. Locate the module you want to remove:

a. Find the module in the module locator diagrams, Figures 6–3, 6–4, and 6–5 (pages 6–14, 6–17, and 6–20, respectively).

b. Note the number of the figure in which you found the module and the module name.

2. If you located the module in Figure 6–3, do the following substeps. If not, skip to step 3.

a. Go to Table 6–4 on page 6–13.

b. Find the procedure that includes the name of the module you want to remove.

c. Perform the instructions in Table 6–4 to access and remove the module.

3. If you have found the module in either Figure 6–4 or Figure 6–5, cabinet removal is required. Do the following substeps:

a. First do *Line Fuse and Line Cord* on page 6–26, removing only the line cord.

b. Then do *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet* on page 6–27, removing only the rear cover and cabinet.

c. Continue with step 4.

4. If you have located the module in Figure 6–4, do the following substeps. If not, skip to step 5.

a. Go to Table 6–5 on page 6–15.

b. Find the procedure that includes the name of the module you want to remove.

c. Perform the instructions in Table 6–5 to access and remove the module.

5. If you have located the module in Figure 6–5, you are removing one of the field replaceable cables. Do the following substeps:

a. Go to Table 6–6 on page 6–18.

b. Find the procedure that includes the name of the cable you want to remove.

c. Perform the instructions in Table 6–6 to access and remove the cable.

Table 6–4: Access Instructions for Modules in Figure 6–3

Procedure Including Module to be Removed	Page No.	Access Instructions
Optical Port Connector	6–22	1 Do only the procedure listed at left.
Front-Panel Knob	6–24	1 Do only the procedure listed at left.
Line Fuse and Line Cord	6–26	1 Do only the procedure listed at left. 2 Remove only the module you want to service.
Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet	6–27	1 Do *Line Fuse and Line Cord* removing only the line cord. 2 Do the procedure listed at left, removing only the module(s) you want to service.
Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets	6–30	1 Do *Line Fuse and Line Cord* removing only the line cord. 2 Do *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*, removing only the rear cover and cabinet. 3 Do the procedure listed at left, removing all modules including the module(s) you want to service.
Plug-In Interface Module	6–33	1 Do the procedure listed at left, removing the module you want to service.
Disk Drive	6–34	1 Do *Line Fuse and Line Cord* removing only the line cord. 2 Do the *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*. 3 Do the procedure listed at left to remove the module.
A06 Front Panel Assembly and Menu Flex Circuit	6–35	1 Do *Disk Drive*. 2 Do *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets*. 3 Do *Plug-In Interface Module*. 4 Do the procedure listed at left, removing all modules including the module(s) you want to service. When doing the procedure listed at left, do not remove the menu flex circuit unless it is being replaced with a new module.

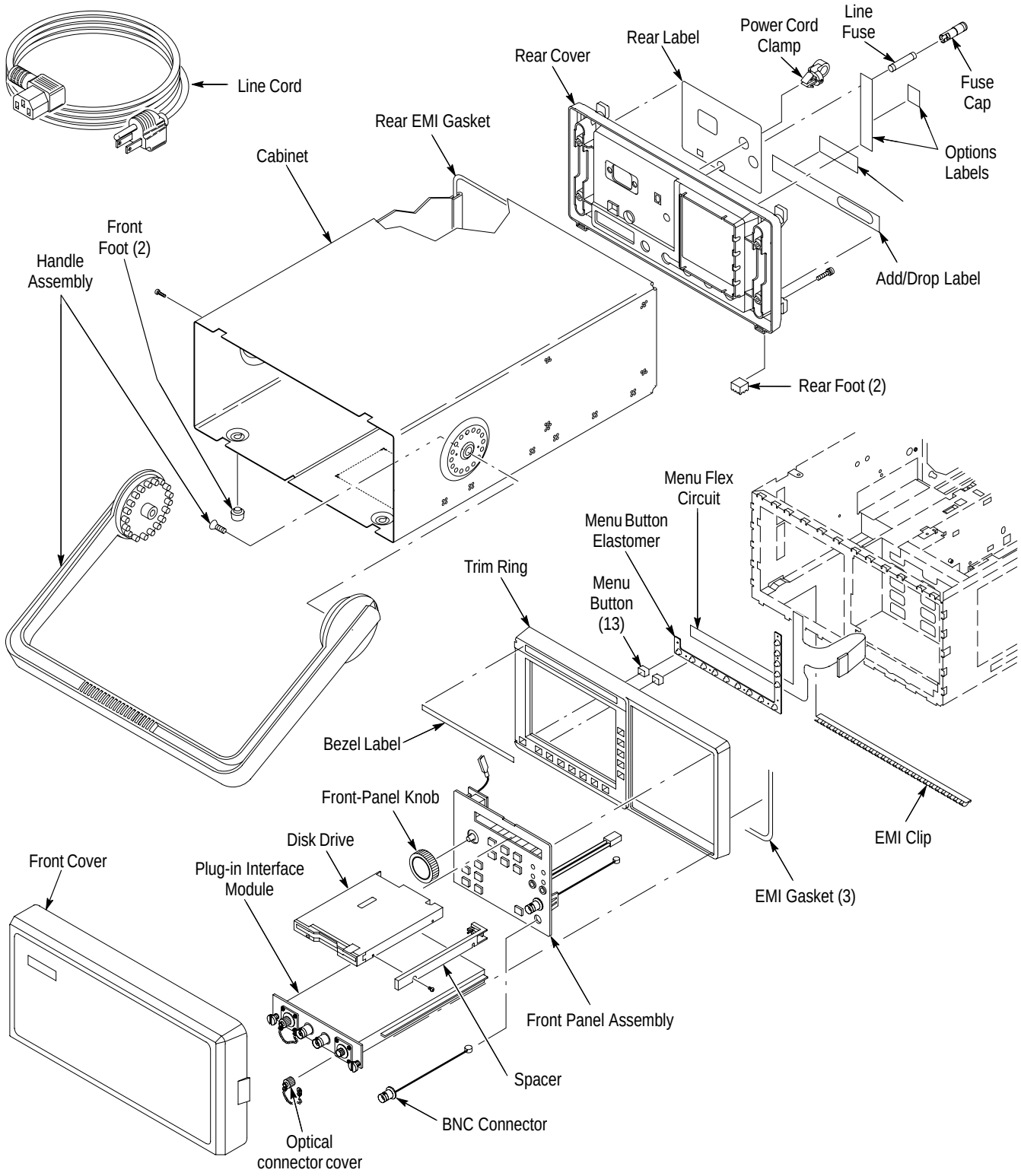

Figure 6–3: Cabinet and Front-Panel Mounted Modules

Table 6–5: Access Instructions for Modules in Figure 6–4

Procedure Including Module to be Removed	Page No.	Access Instructions
A10 High Speed Protocol Assembly	6–39	1 Do the procedure listed at left to remove the module.
A09 Main Protocol Assembly	6–41	1 Do *Com Bus, Board Supports, and PCAT Bus*, removing only the Com Bus and the PCAT Bus. 2 Do *Plug-In Interface Module*. 3 Do *A10 High Speed Protocol Assembly*. 4 Do the procedure listed at left to remove the module.
A26 Monitor Assembly	6–42	1 Do the procedure listed at left to remove the module.
Com Bus, Board Supports, and PCAT Bus	6–45	1 Do the procedure listed at left to remove the module.
EMI Shield	6–46	1 Do the procedure listed at left to remove the module.
A03 CPU Assembly	6–47	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A01 Display Assembly	6–49	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A08 Clock Generator Assembly	6–50	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
Tributary Assembly	6–51	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A12/A14 JAWA/JAWG Assembly	6–53	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A02 Backplane Assembly	6–55	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the card-cage board procedures: *A03 CPU Assembly*, *A01 Display Assembly*, *A08 Clock Generator Assembly*, and *Tributary Assembly*. 4 Do the procedure listed at left to remove the module.

Table 6–5: Access Instructions for Modules in Figure 6–4 (Cont.)

Procedure Including Module to be Removed	Page No.	Access Instructions
Back-Up Battery	6–56	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the card-cage board procedures: *A03 CPU Assembly*, *A01 Display Assembly*, *A08 Clock Generator Assembly*, and *Tributary Assembly*. 4 Do the procedure listed at left to remove the module.
Fan and Fan Mount	6–58	1 Do the procedure listed at left to remove the module.
A25 Low Voltage Power Supply and its Mount	6–60	1 *Only* if removing the plastic mount that secures the Low Voltage Power Supply, do all the procedures necessary to remove the *A02 Backplane Assembly*. 2 Do procedure *Fan and Fan Mount*. Do not remove the fan mount. 3 Do the procedure listed at left to remove the module.
A07 Auxiliary Power Supply	6–62	1 Do the procedure listed at left to remove the module.
Line Filter	6–63	1 Do the procedure listed at left to remove the module.

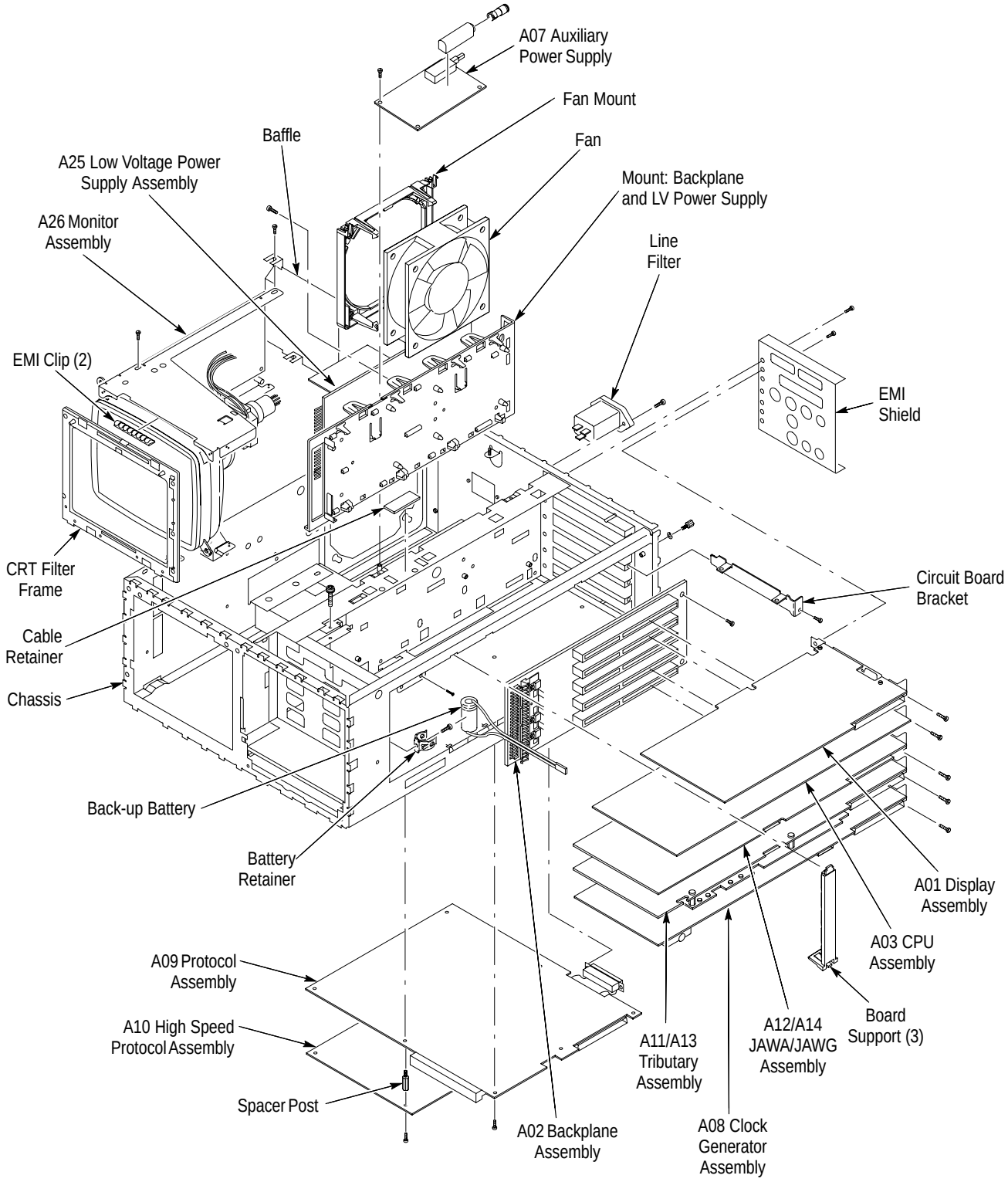

Figure 6–4: Internal Modules

Table 6–6: Access and Removal Instructions for Cables in Figures 6–5 and 6–6

Name of Cable	Access and Removal Instructions
Disk Drive-to-Display	1 Lift up on the latch at each side of both jacks. 2 Unplug the cable to be replaced from the disk drive and A03 CPU assemblies. See Figure 6–5 for jack location. 3 Reverse these instructions to install the replacement cable.
PCAT Bus	1 Unplug the cable to be replaced from the A01 Display and A09 Main Protocol assemblies. See Figure 6–5 for jack location. 2 Reverse these instructions to install the replacement cable.
Com Bus	1 Follow the procedure for removing the PCAT Bus. 2 Unplug the cable to be replaced from the board assemblies. See Figure 6–5 for board locations. 3 Reverse these instructions to install the replacement cable.
CPU-to-Front Panel	1 Find the procedure *A06 Front Panel Assembly and Menu Flex Circuit* in Table 6–5. 2 Follow the access instructions found there to access and remove the A06 Front Panel assembly. The cables plugged into that assembly will be removed in the process. 3 Unplug the cable to be replaced from the A03 CPU assembly. See Figure 6–5 for jack location. 4 Reverse these instructions to install the replacement cable.
Main Protocol-to-Clock Generator	1 Find the procedure *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet* in Table 6–5. 2 Follow the access instructions found there to access and remove the rear panel and cabinet. 3 Unplug the Com Bus cable from the A09 Main Protocol and A08 Clock Generator assemblies. See Figure 6–5 for jack locations. 4 Reverse these instructions to install the replacement cable.
Backplane-to-Low Voltage Power Supply-to-Main Protocol	1 Reach in from the top of the CTS 700-Series Test Set and unplug the cable at the jacks at the front of the backplane and Low-Voltage Power Supply modules. 2 Set the CTS 700-Series Test Set so its top is down. Unplug the cable to be replaced from the A09 Main Protocol assembly. See Figure 6–5 for jack locations. 3 Reverse these instructions to install the replacement cable.

Table 6–6: Access and Removal Instructions for Cables in Figures 6–5 and 6–6 (Cont.)

Name of Cable	Access and Removal Instructions
Auxiliary Power Supply-to-Line Filter *Auxiliary Power Supply-to-Low Voltage Power Supply*	1 Find the procedure *A07 Auxiliary Power Supply* in Table 6–5. 2 Follow the access instructions found there to access and remove the Auxiliary Power Supply assembly. 3 Use a 15 W soldering iron to unsolder the cable from the Auxiliary Power Supply. 4 Reverse these instructions to install the replacement cable.
Auxiliary Power Supply-to-Low Voltage Power Supply-to-Ground Lug *Line Filter-to-Ground Lug*	1 If removing the Auxiliary Power Supply-to-Low-Voltage Power Supply-to-ground lug cable, unplug the cable from the Low-Voltage Power Supply and use a 15 W soldering iron to unsolder the cable from the Auxiliary Power Supply. 2 If removing the line filter-to-ground lug cable, unplug it from the line filter lug. See Figure 6–5. 3 Using a 5/16 inch nut driver (Item 8) remove the nut(s) that secure the cable to be removed from the lug and remove it. 4 Reverse these instructions to install the replacement cable.
Monitor	1 Find the procedure *A01 Display Assembly* in Table 6–5. 2 Follow the access instructions found there to access and remove the display assembly. The cable will be unplugged from that assembly in the process. 3 Unplug the cable from the monitor. See Figure 6–5 for jack location. 4 Unplug the cable from the Auxiliary Power Supply. See Figure 6–5 for jack location. 5 Reverse these instructions to install the replacement cable.

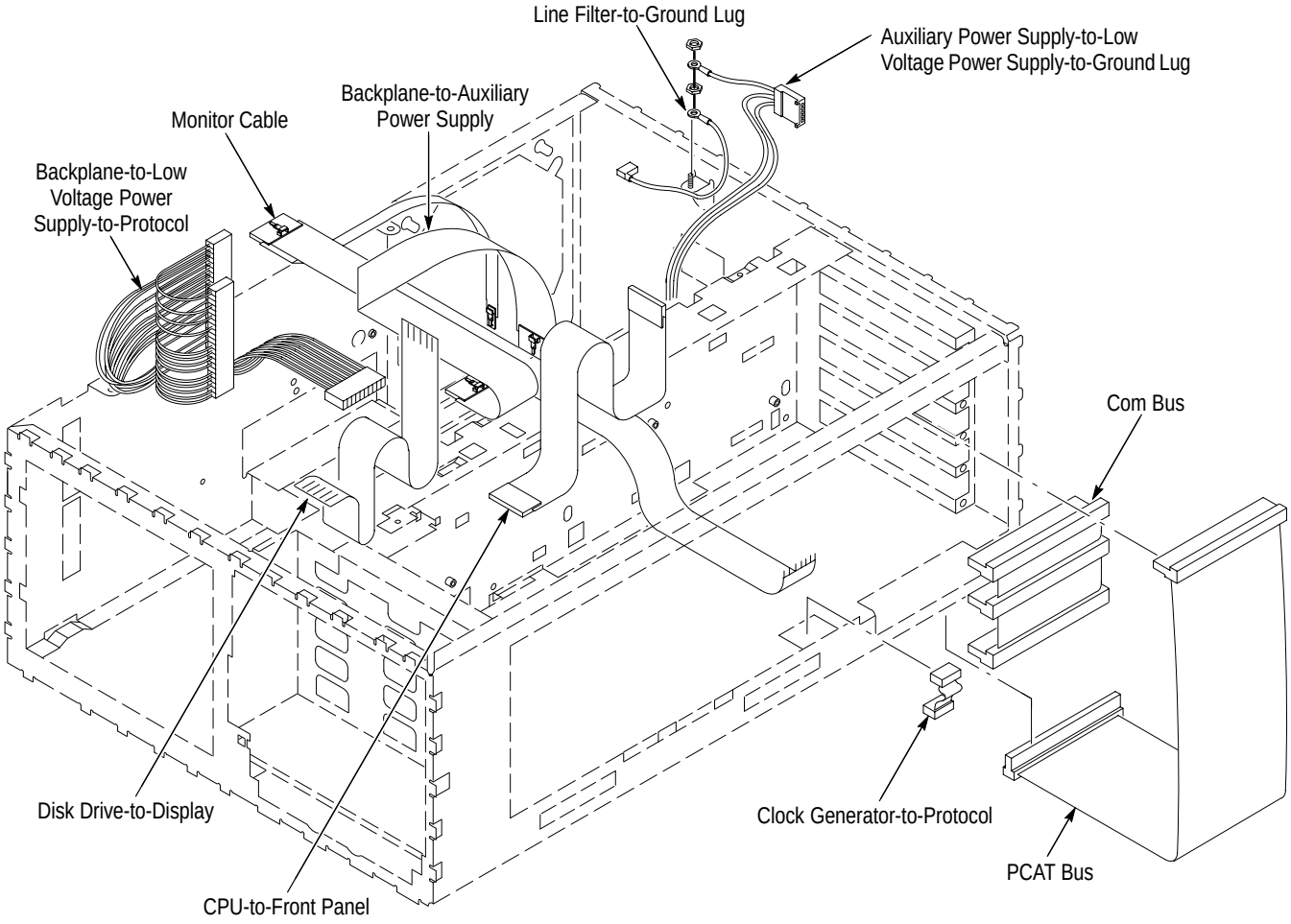

Figure 6–5: CTS 710 Cables and Cable Routing

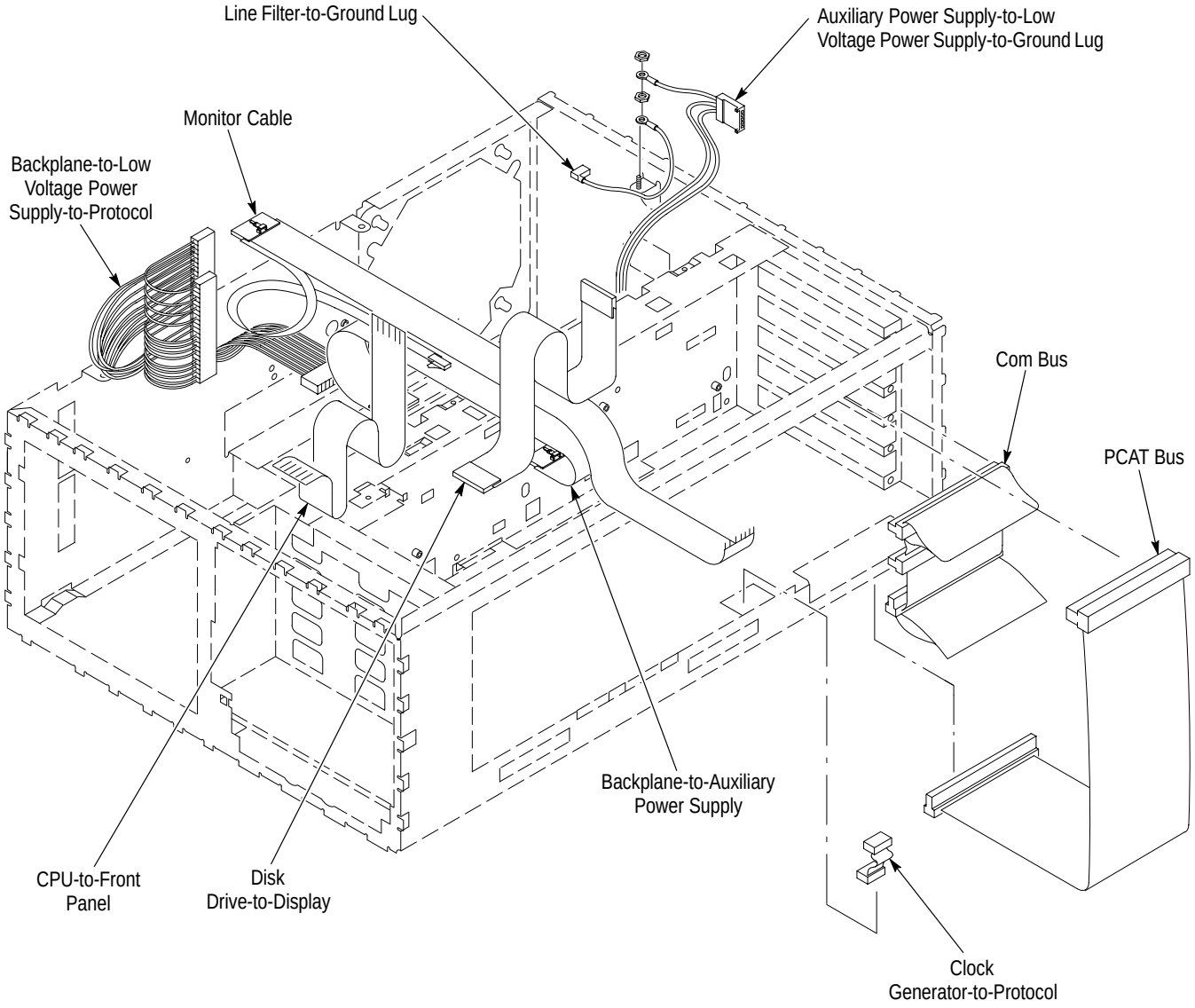

Figure 6–6: CTS 750 Cables and Cable Routing

Procedures for Module Removal and Installation

Do the *Access Procedure* (page 6–11) before doing any procedure in this collection.

Optical Port Connector

The CTS is shipped with the FC connector bulkhead and dustcap installed. If you wish to replace the connector or change to the ST, DIN 47256, or SC connectors perform the following procedure:

1. Verify that the CTS has been turned off with the principal power switch on the rear panel.
2. Remove the four screws that attach the bulkhead connector to the front panel (see Figure 6–1, page 6–5).
3. Gently pull the bulkhead out of the unit and unscrew the fiber connector. Be careful not to pull beyond the fiber slack.
4. Disassemble the bulkhead as shown in Figures 6–7 through 6–10.

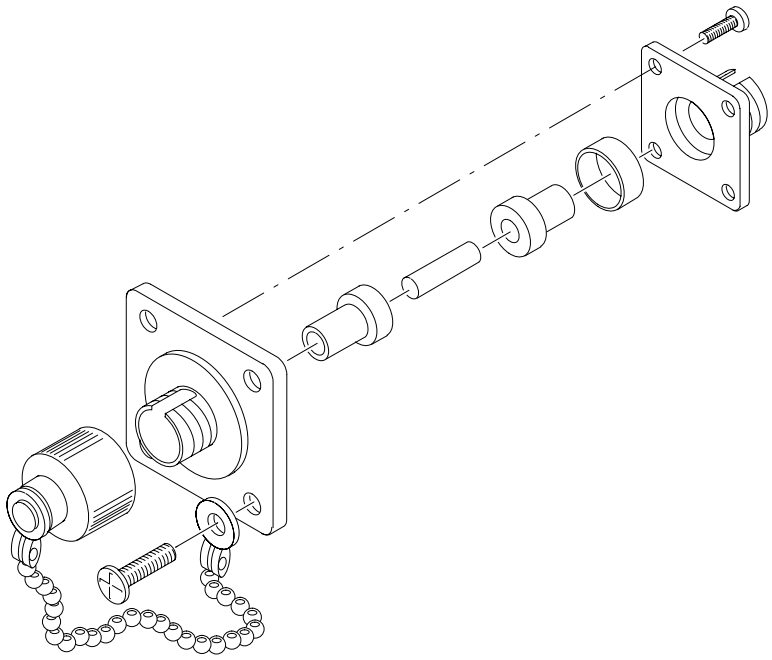

Figure 6–7: FC Optical Bulkhead Assembly

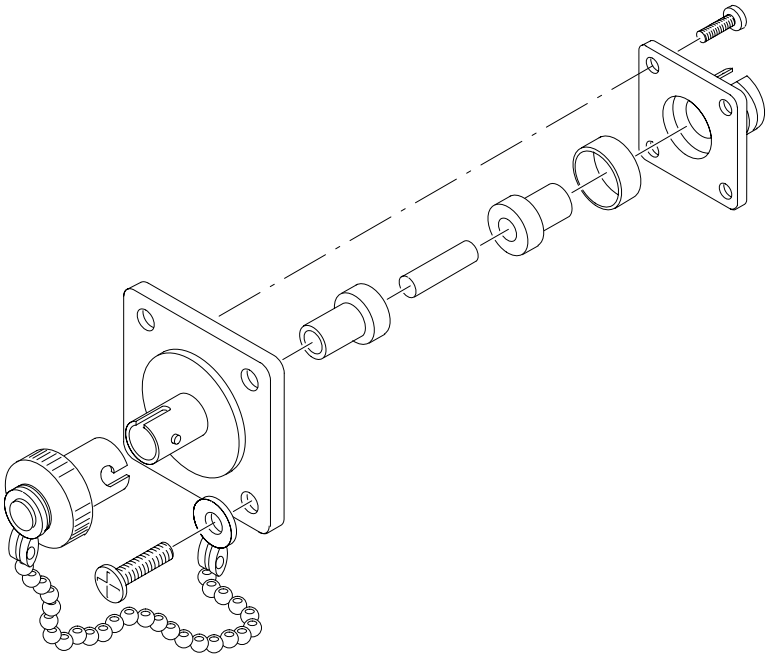

Figure 6–8: ST Optical Bulkhead Assembly

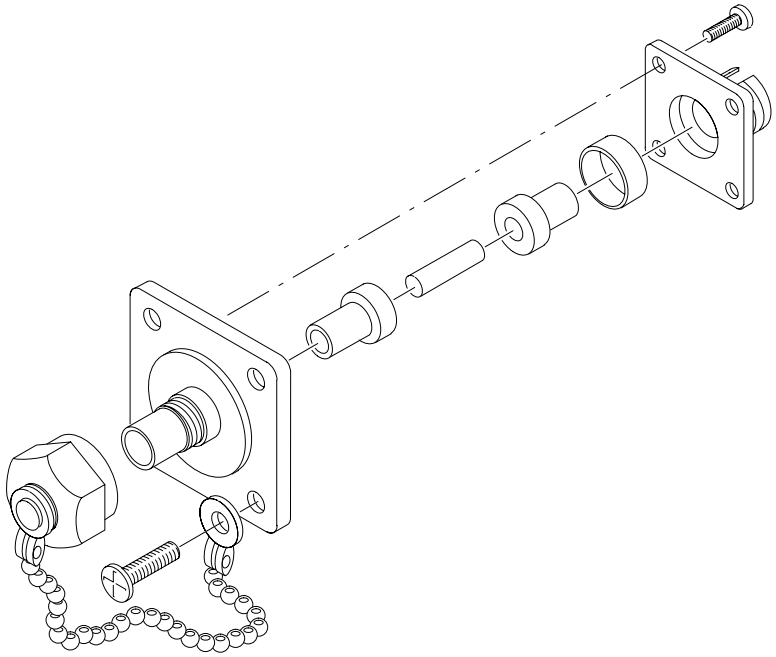

Figure 6–9: DIN 47256 Optical Bulkhead Assembly

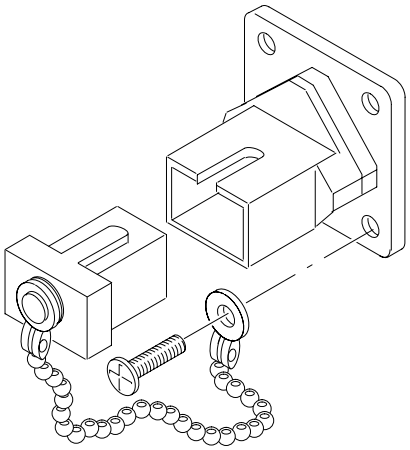

Figure 6–10: SC Optical Bulkhead Assembly

5. Replace the current bulkhead with the one you wish to use and re-assemble.
6. The final part of installation is the reverse of steps 1 through 3.

Front-Panel Knob

For this procedure you will need a 1/16 inch hex key screwdriver (item 12).

1. Set the CTS so its bottom is down on the work surface and its front is facing you.
2. To remove the knob, loosen the Allen screw in the side of the knob (see Figure 6–11).
3. To reinstall, hold the knob in place and tighten the Allen screw. Be sure the knob is not scraping against the front panel.

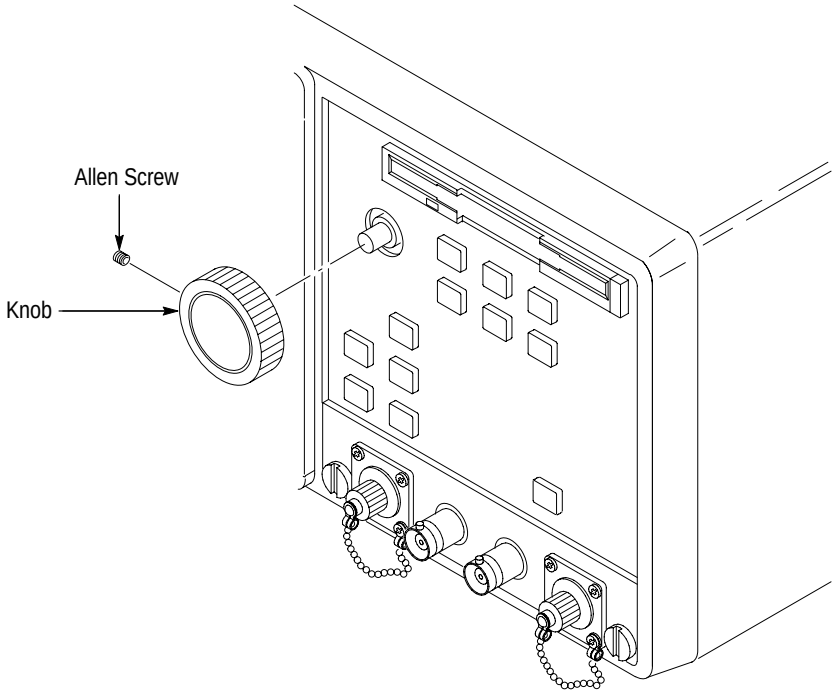

Figure 6–11: Knob Removal

Line Fuse and Line Cord

For this procedure you will need a flat-bladed screwdriver (item 4).

WARNING. *Unplug the line cord from the line voltage power source before continuing. Failure to do so can cause death or injury.*

1. Locate the line fuse and line cord in Figure 6–12.
2. Set the CTS so its bottom is down on the work surface and its rear is facing you. If you are servicing the line cord, do the next step; if you are servicing the line fuse, skip to step 4.

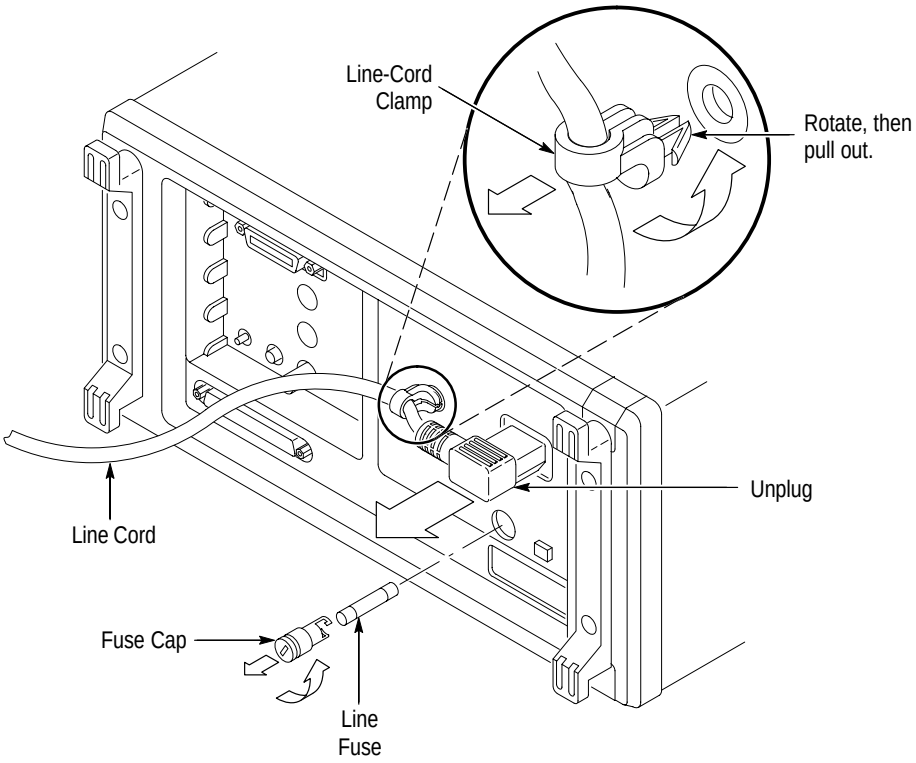

Figure 6–12: Line Fuse and Line Cord Removal

3. To remove the line cord, unplug it from the CTS, rotate the line-cord clamp 90° counterclockwise, and then remove the assembly from the CTS.
4. To remove the line fuse, turn the fuse cap counterclockwise using a flat-bladed screwdriver.
5. To reinstall the line fuse and line cord, do steps 4 and 3 in reverse.

Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet

For this procedure you will need a screwdriver with size T-15 and T-20 Torx® tips (items 1, 2, and 3) and a flat-bladed screwdriver (item 4). If removing the EMI gasket at the inside rear of the cabinet, you will also need a pair of needle-nose pliers (item 5).

1. Make sure the CTS front cover is installed; if not, install it by snapping its edges over the trim ring.
2. Rotate the handle toward the bottom of the CTS, and then set the CTS front down on the work surface with the bottom facing you (see Figure 6–13).
3. If removing a front foot for replacement, use a pair of slip-jaw pliers to firmly grip the foot, and then pull with a turning motion to remove. Reverse the process to install the replacement foot.
4. To remove the rear cover, remove the four T-15 Torx-drive screws securing the rear cover to the CTS. Lift off the rear cover. If no other modules are being serviced, skip to the end (step 9) of this procedure.
5. If removing a rear foot for replacement, use a flat-bladed screwdriver to press the foot out from inside the rear cover. Use your hand to press a replacement foot into the rear cover. If no other modules are being serviced, skip to the end (step 9) of this procedure.
6. To remove the cabinet, perform the following steps:
   a. Remove the single T-15 Torx-drive screw at the left side of the CTS.
   b. Grasp the two handle hubs and pull them outward as if to rotate the handle.
   c. While holding the handle hubs pulled out, lift the cabinet upwards to slide the cabinet off the CTS.
   d. At the rear of the cabinet, grasp its left and right edges. Take care not to bind or snag the cabinet on the internal cabling as you remove the cabinet.
   e. If no other cabinet modules are being serviced, skip the rest of this procedure.

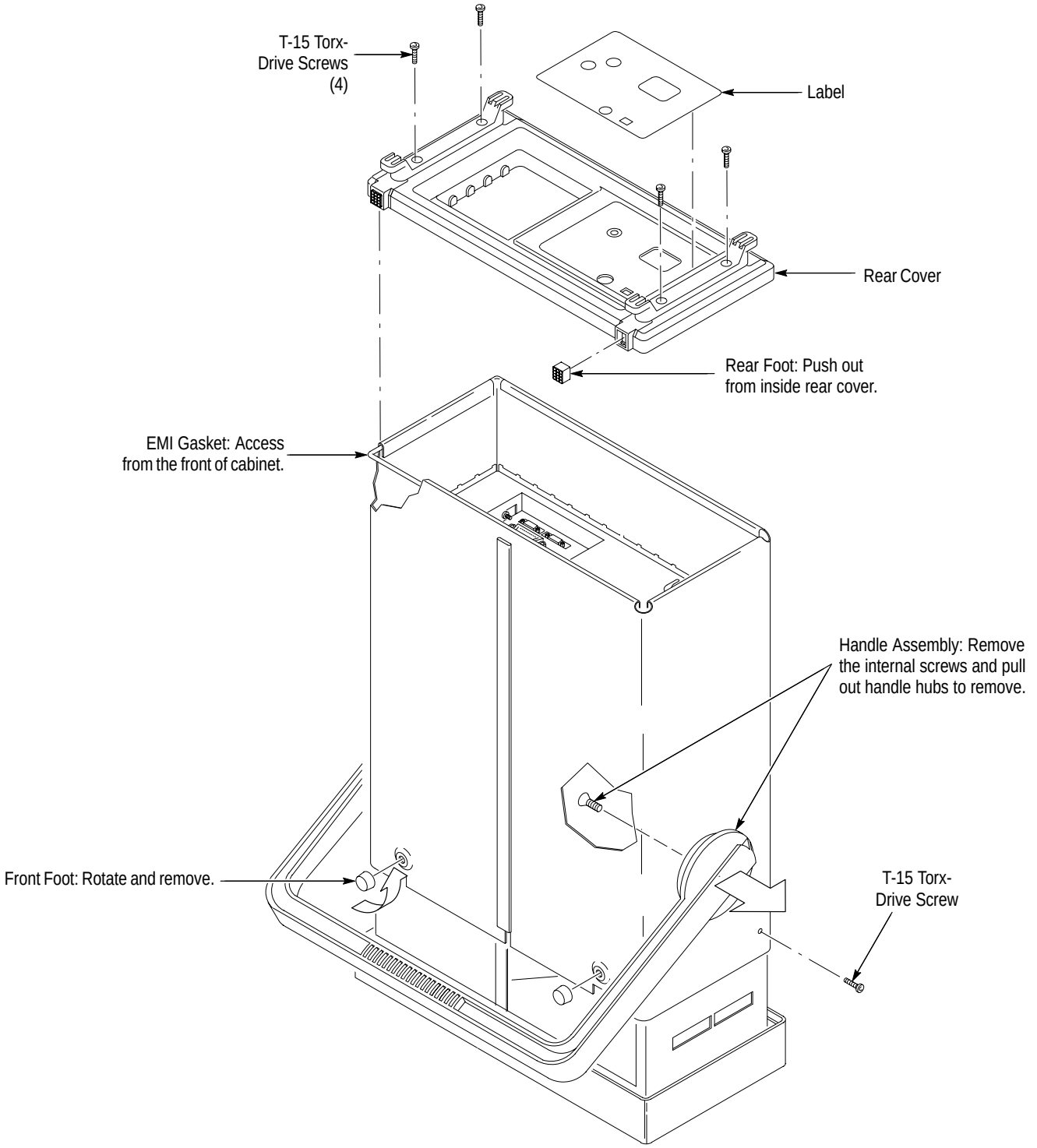

Figure 6–13: Front Cover, Rear Cover, Cabinet, EMI Gasket, and Cabinet Handle and Feet Removal

7. If removing the handle assembly for cleaning or replacement, perform the following steps:

   a. Working from the inside of the cabinet, remove the T-20 Torx-drive screw securing each handle hub to the cabinet.

   b. Working from the outside of the cabinet, grasp the two handle hubs and pull them outward from the cabinet until they are out of the cabinet.

   c. While holding the handle hubs pulled out, lift the handle away to remove.

***NOTE**. DO NOT do step 8 to remove the EMI gasket from the rear of the cabinet unless it must be replaced due to damage. If you are not replacing that gasket, skip to step 9.*

When reinstalling the EMI gasket and the CTS cabinet, carefully follow the instructions given. Unless they are performed properly, the CTS may not meet its emissions requirements (EMI).

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8. If removing the EMI gasket for replacement, perform the following steps:

   a. Locate the EMI gasket to be removed in the diagram *Front Cover, Rear Cover, Cabinet, EMI Gasket, and Cabinet Handle and Feet Removal*, Figure 6–13.

   b. Look for the point where the ends of the gasket touch in the channel at the rear edge of the cabinet.

   c. Use a pair of needle-nose pliers to pry up one of the ends of the gasket.

   d. Grasp the EMI gasket, and gently pull it out of its channel.

9. To reinstall the cabinet and rear cover, perform the following steps:

   a. If the EMI gasket was removed, press the new EMI gasket into its groove at the rear edge of the cabinet. Make sure the ends of the gasket touch, but do not overlap. (Cut off excess length if required to prevent overlap.)

   b. See step 7 to reinstall the handle assembly (if it was removed).

   c. Do step 6 in reverse order to reinstall the cabinet, while observing the following precautions and requirements:

      - Take care not to bind or snag the cabinet on internal cabling; dress cables as necessary.

- When sliding the cabinet onto the CTS, be sure the ridge around the rear of the main chassis slides into the groove containing the EMI gasket on the rear of the cabinet.
- Install the four screws at the rear panel, and tighten to 8 inch-lbs torque before installing the single screw at the left side of the cabinet. Tighten this screw to 8 inch-lbs.

d. See step 5 to reinstall the rear cover. If installing a new rear cover, also do the following:

- Find the appropriate labels for your rear cover.
- Remove the covering from the back of the sticky-back label, align it to the rear cover, and press firmly to install.

Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets

For this procedure you will need a spudger (item 13).

1. Set the CTS so its rear is down on the work surface and its bottom is facing you (see Figure 6–14).
2. If the front cover is installed, remove it by grasping its left and right edges and snapping it off the front of the CTS.

CAUTION. *Do not touch the carbon contact points on the menu elastomer installed in the trim ring. Also, do not touch the contacts on the menu button flex circuit exposed when you remove the trim ring. You should wear clean cloth gloves that are free of lint when handling the menu elastomer or when touching the menu button flex circuit mounted on the front chassis.*

3. To remove the trim ring, pull the top flex locks outward, and then lift the top of the trim ring forward to snap it loose from the main chassis. Repeat the process to loosen the bottom edge of the trim ring. When removed, lay the trim ring on its face on the work surface.
4. To remove the front EMI gaskets, lift them out of the trim ring.
5. If servicing the menu elastomer, lift it out of the trim ring.
6. If servicing the menu buttons, lift them out of the trim ring.

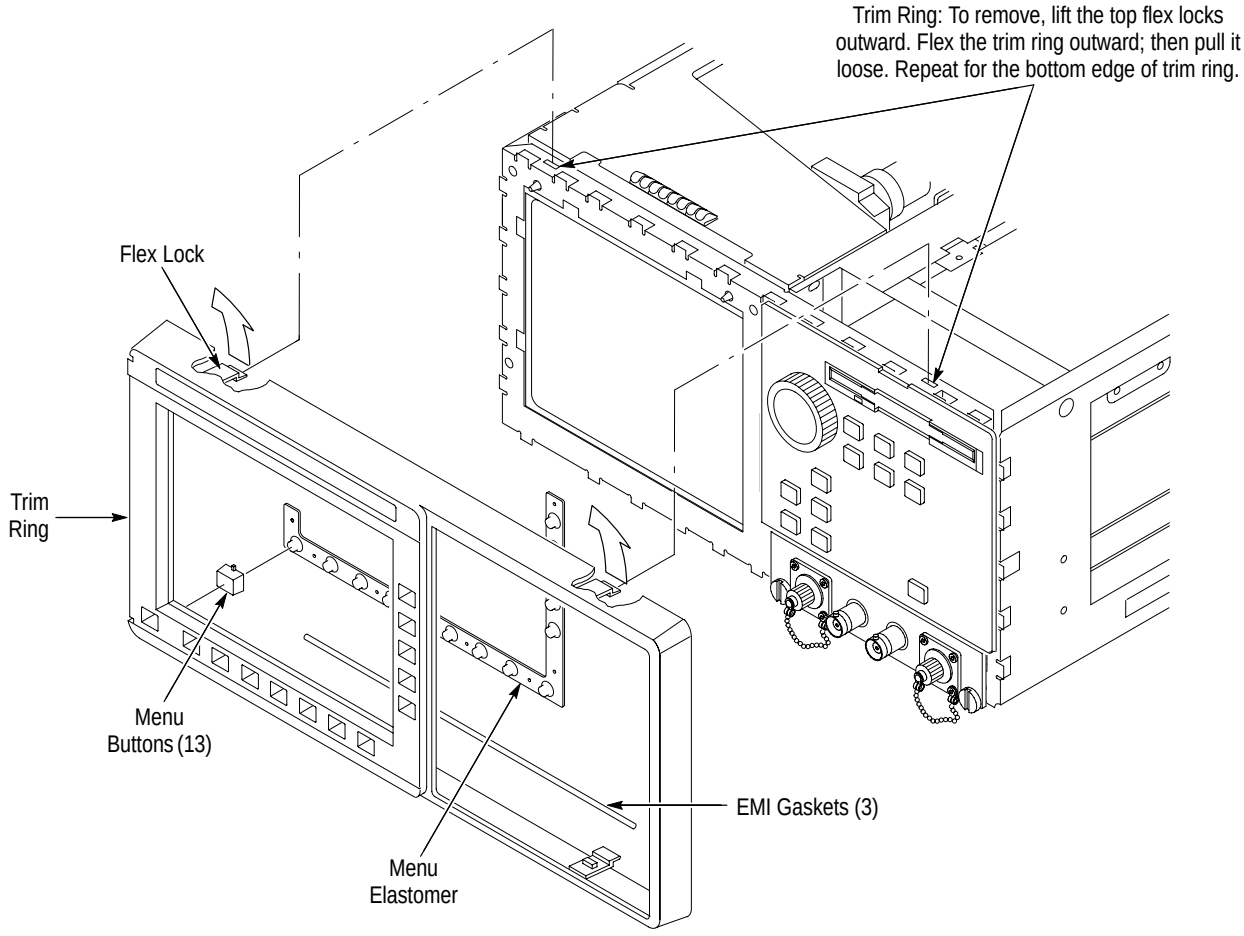


Figure 6–14: Trim Ring, Menu Elastomer, and Menu Buttons Removal

7. To reinstall the trim ring, perform the following steps:

a. If the menu buttons were removed, insert each button into its hole in the trim ring.

b. If the menu elastomer was removed, align it over the menu button holes in the trim ring, and press it in to install. Avoid touching the carbon contact points on the elastomer when installing.

c. Without installing the EMI gaskets, align the trim ring to the front of the chassis, and push it on to seat. Be sure that both pairs of flex locks, one pair each at the inside top and bottom of the trim ring, snap over the edge of the chassis.

8. To reinstall the EMI gaskets, perform the following steps (see Figure 6–15):

a. Install the front cover on the CTS.

b. Lay the CTS so its front cover is on the work surface.

c. Align an EMI gasket so it lays in the groove between the trim ring and the chassis between the top pair of flex locks.

d. Using a spudger, push the EMI gasket until it is firmly seated at the bottom of the groove. It should not overlap either flex lock.

e. Repeat the process just described to install the remaining two side gaskets.

9. If the trim ring installed in step 7 is a new trim ring, also do the following:

a. Find the label that matches your model CTS (CTS 710 or CTS 750).

b. Remove the covering from the back of the sticky-back label, align it to the trim ring, and press firmly to install.

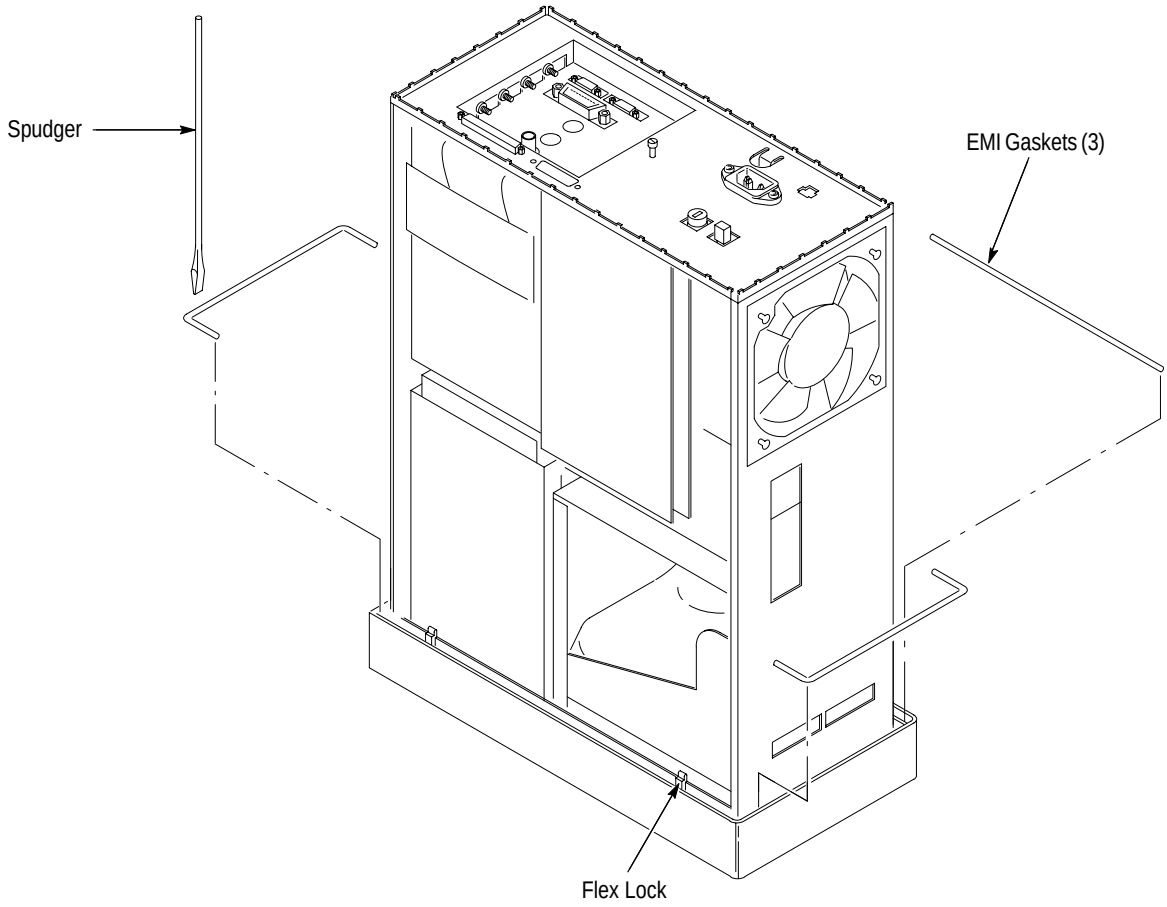


Figure 6–15: EMI Gasket Installation

Plug-In Interface Module

For this procedure you will need a flat-bladed screwdriver (item 4).

1. Set the CTS so its bottom is down and its front is facing you.
2. To remove the Plug-In Interface Module, perform the following steps using Figure 6–16 as a guide:
   a. If not already installed, screw the dust caps onto the optical connectors.
   b. Using a screwdriver, loosen the two screws on the front panel of the module.
   c. Grasp the module by its two front-panel screws, and slide the module out of the front panel to complete its removal.

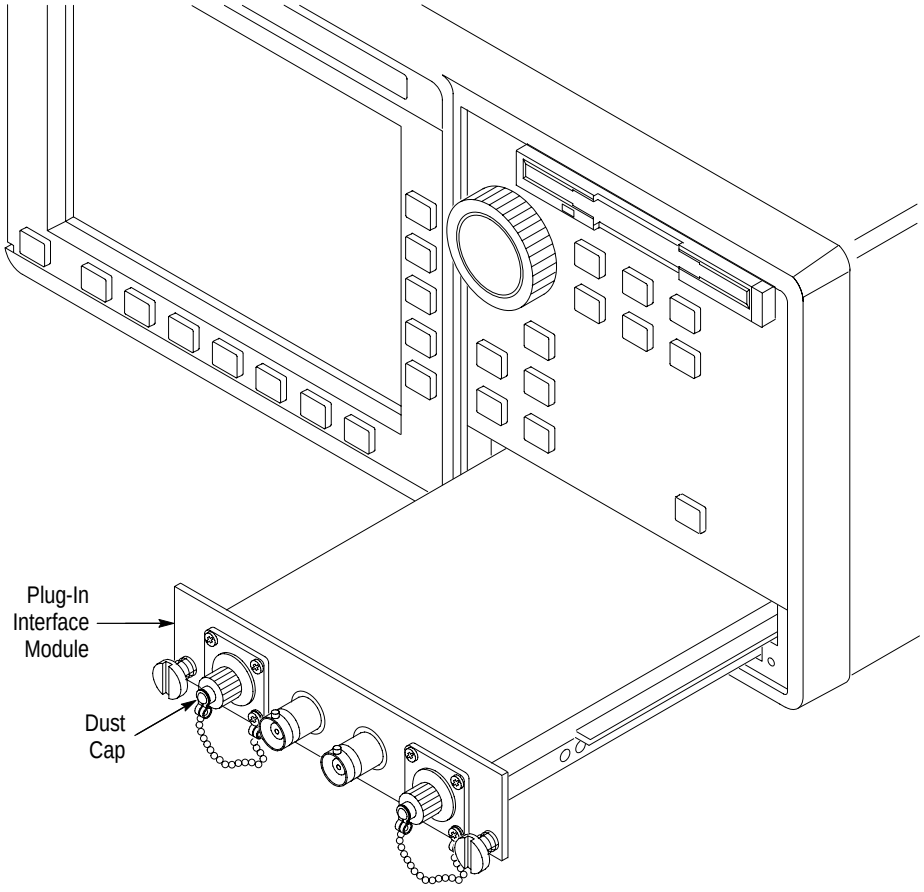


Figure 6–16: Cabinet and Front-Panel Mounted Modules

3. To reinstall the Plug-In Interface Module, perform the following steps:

   a. Align the Plug-In Interface module edges with the guides, and then slide it into the cavity of the CTS.

   b. Using both thumbs, press on the Plug-In Interface Module front panel until the module is completely seated in the CTS.

   c. With the screwdriver, tighten each thumbscrew until snug.

Disk Drive

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2) and a Pozidriv screwdriver (item 7).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down and its front is facing you.

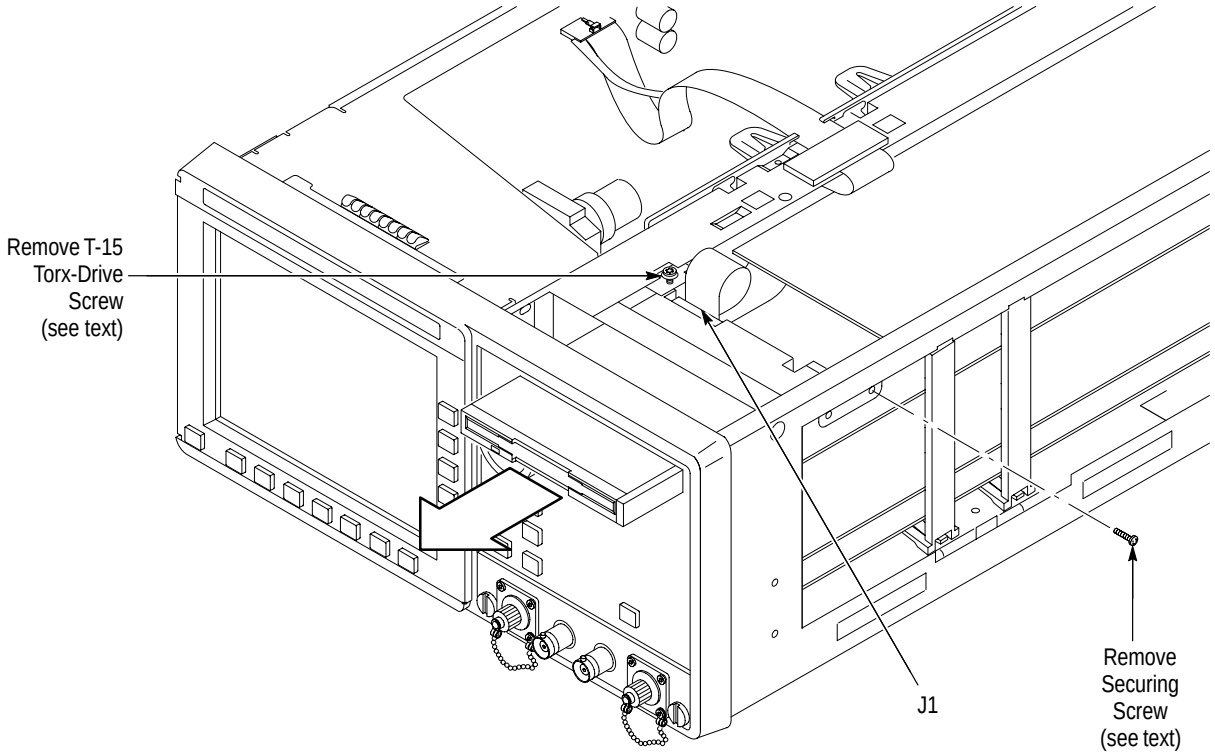


Figure 6–17: Disk Drive Removal

3. To remove the disk drive, perform the following steps using Figure 6–17 as a guide:

   a. Lift up on the two locking tabs on J1 of the disk drive.

b. Remove the cable from the drive.

c. If present, remove the T-15 Torx-drive screw that clamps the drive in the chassis. When replacing the drive, do not reinstall this screw.

d. Remove the one or two screws securing the drive to the chassis.

e. Grasp the drive by its front edges, and pull it out of the front panel to complete its removal.

f. If present, remove the screw securing the spacer to the drive, and lift the spacer away from the drive to complete the removal.

4. To reinstall the disk drive, perform steps 3a–3f in reverse order.

A06 Front Panel Assembly and Menu Flex Circuit

For this procedure you will need a flat-bladed screwdriver (item 4) and hex key screwdriver (item 12).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down on the work surface and its front is facing you.

3. To remove the A06 Front Panel assembly, perform the following steps using Figure 6–18 as a guide:

a. If your CTS contains the optional Add/Drop/Test connectors, unplug the following cables (your CTS may not contain all three cables) from their jacks on the Tributary assembly (J225, J217, J218, and J220 on Option 22; J225, J5, J6, and J7 on Option 36).

b. Insert a flat-bladed screwdriver (item 4) into the slot at the front right of the chassis. Push inwards to release the snap lock at the right side.

c. While guiding the Add/Drop cables, if any, through the chassis access holes, lift the A06 Front Panel assembly out of the front of the main chassis until you can reach the interconnect cables connecting it to various other modules.

d. Unplug the following cables from their jacks on the A06 Front Panel assembly:

- The CPU-to-front-panel cable at J101
- The menu flex circuit at J301
- The ground cable to chassis ground lug

e. Finally, lift the A06 Front Panel assembly out of the front of the main chassis to complete the removal.

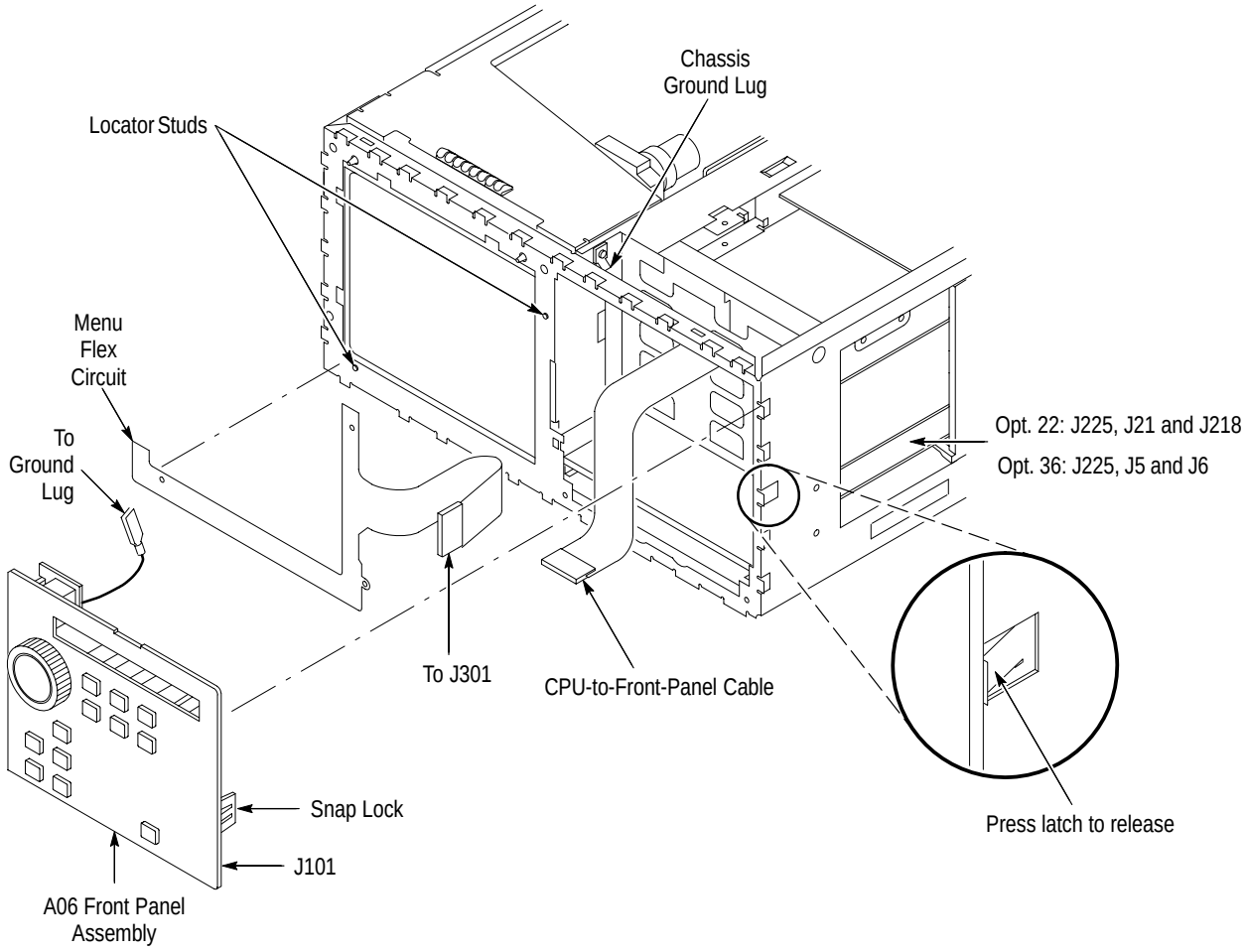


Figure 6–18: A06 Front Panel Assembly and Menu Flex Circuit Removal

***NOTE**. Perform step 4 only if disassembling for cleaning and lubrication. (Components removed in step 4 are not field replaceable.) Otherwise, skip to step 5 to continue this procedure.*

4. If the front panel or the front-panel buttons are to be cleaned, perform the following steps:

a. Remove the knob from the A06 Front Panel assembly using the method described in *Front-Panel Knob* on page 6–24.

b. Release the four snap locks at the edge of the circuit board and the snap lock near the center of the circuit board, and then lift the board away from the assembly (see Figure 6–19).

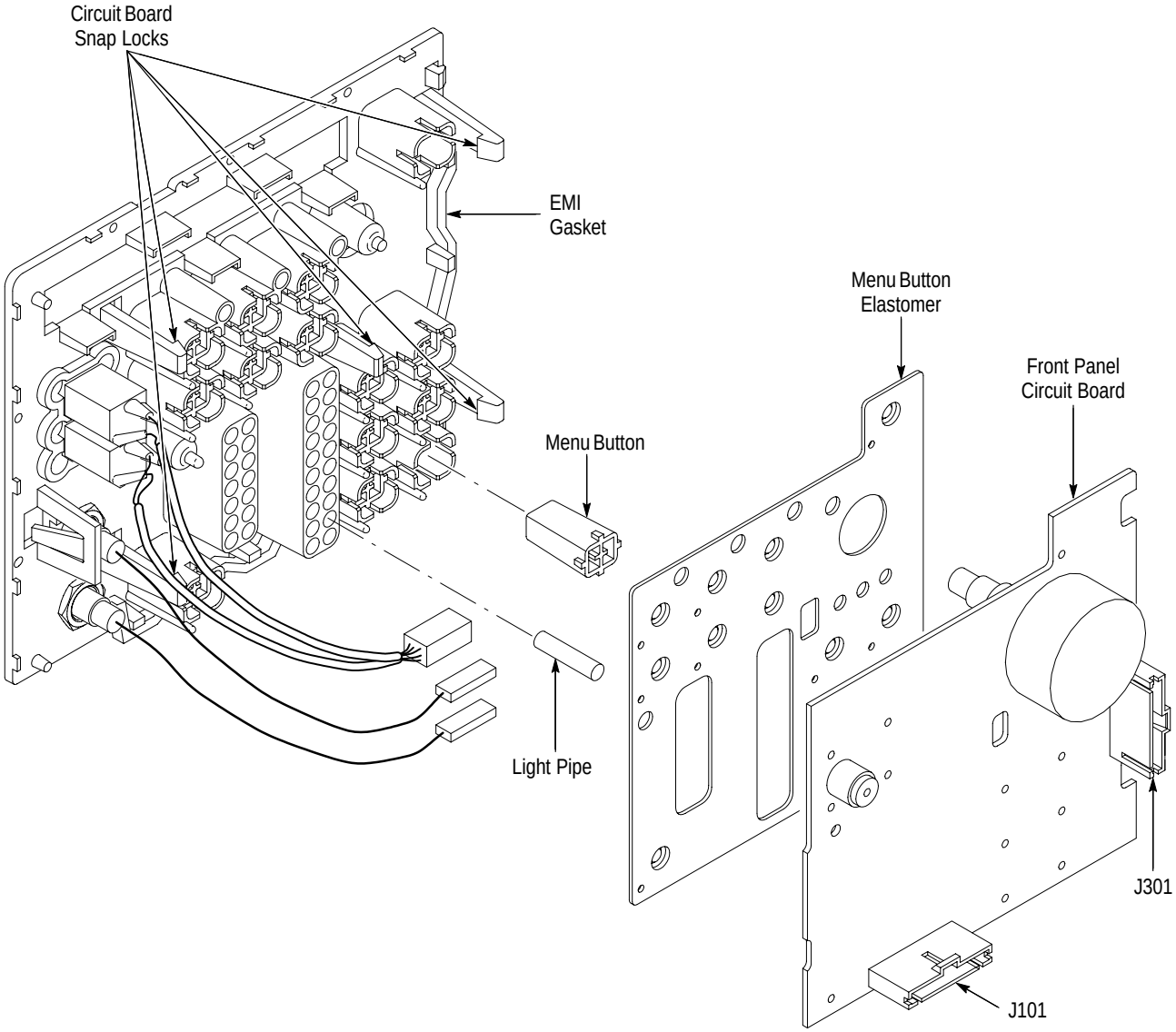


Figure 6–19: Disassembly of the Front Panel Assembly

c. Disassemble the front-panel-assembly components using Figure 6–19 as a guide. During disassembly, be careful not to spill the light pipes from their sockets; the light pipes are not attached and can slide out easily.

d. Reverse the procedure to reassemble.

CAUTION. *Perform step 5 only if replacing a failed or damaged menu flex circuit with a new unit from the factory. (Removal of the circuit is likely to destroy it.) If this is not the case, skip to step 7 to continue this procedure.*

5. To remove the menu flex circuit, perform the following steps:

a. Slowly pull the flex circuit away from the front of the main chassis. (Removing the flex circuit slowly helps keep the adhesive backing from sticking to the chassis.)

b. Wipe the front of the chassis using isopropyl alcohol and a clean, lint-free cloth. Make sure to remove any adhesive left over from the old flex circuit. Let dry.

6. To install a new menu flex circuit, perform the following steps:

a. Do not touch the contacts on the menu flex circuit with your bare fingers. You should wear clean cloth gloves that are free of lint when installing the menu flex circuit on the front chassis.

b. Find the score line in the adhesive backing and peel the backing off the menu flex circuit.

c. Carefully align the three holes on the menu flex circuit to the locator studs on the front of the main chassis. (See Figure 6–18.) When the alignment is correct, press the flex circuit against the chassis so it adheres to the chassis.

d. Clean the surface of the menu flex circuit just installed using isopropyl alcohol and a clean, lint-free cloth.

7. To reinstall the A06 Front Panel assembly, perform steps 3a–3d in reverse order. Be sure to dress the CPU-to-front-panel cable so that the loop of extra cable length is in the front-panel cavity of the chassis, as shown in Figure 6–5 on page 6–20.

A10 High Speed Protocol Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its top is down and its left side is facing you.
3. To remove the A10 High Speed Protocol board, perform the following steps using Figure 6–20 as a guide:
   a. Remove the four T-15 Torx-drive screws securing the board to the chassis.
   b. Grasp the board by its edges, and pull upward to unplug it from the A09 Main Protocol assembly.
   c. Lift the board away from the chassis to complete its removal.
4. To reinstall the A10 High Speed Protocol board, perform steps 3a–3c in reverse order.

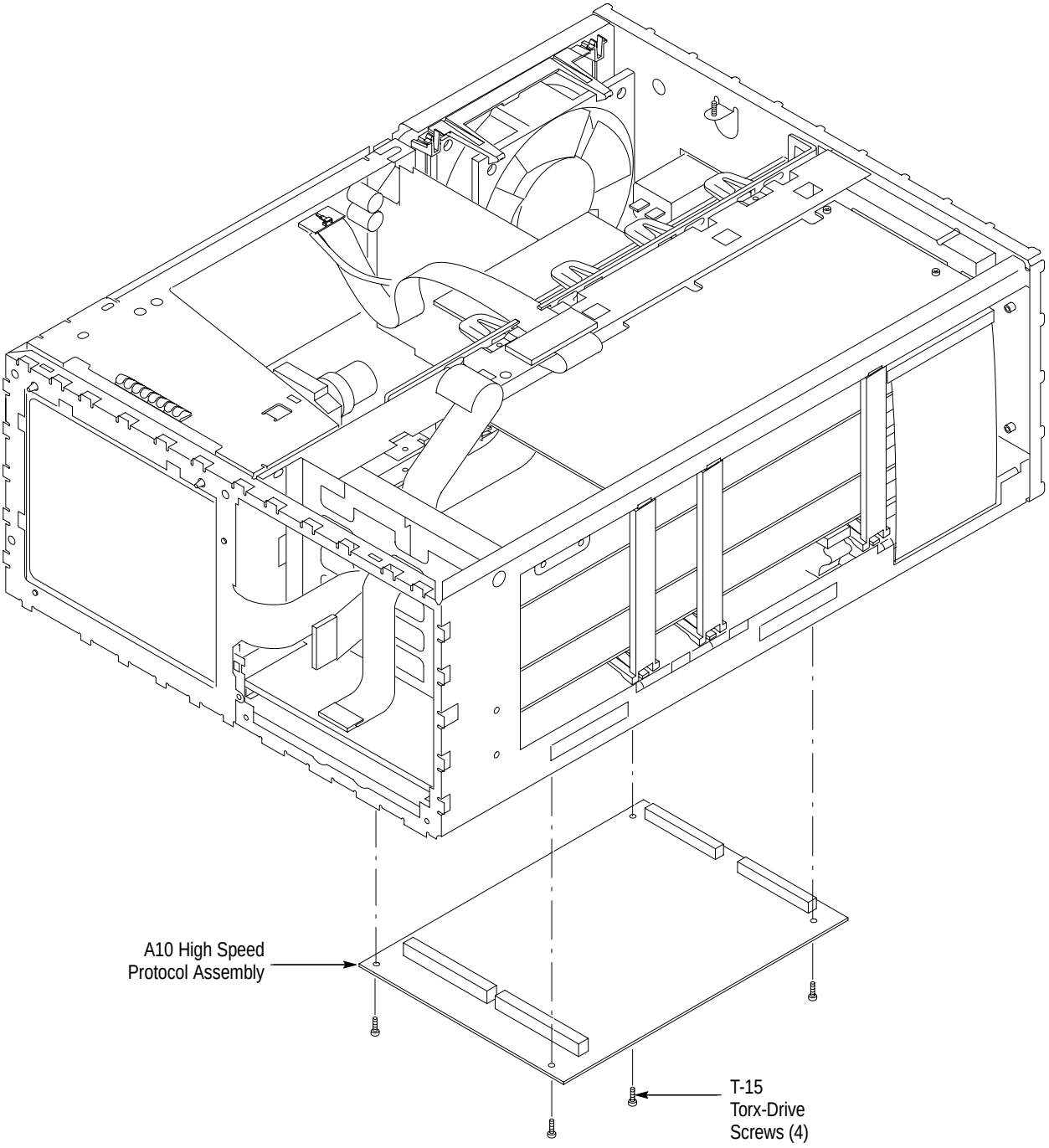


Figure 6–20: A10 High Speed Protocol Assembly Removal

A09 Main Protocol Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2) and 3/16 inch and 1/4 inch nut drivers (items 9 and 10).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its right side is up, with its bottom facing you.
3. To remove the A09 Main Protocol assembly, perform the following steps using Figure 6–21 as a guide:
   a. Unplug the cable from the low voltage power supply assembly from J15.
   b. Unplug the cable from the A08 Clock Generator assembly from J930.
   c. Remove the two 3/16 inch screws securing the Overhead Add/Drop connector to the rear panel.
   d. Remove the four 1/4 inch spacer posts securing the A09 Main Protocol assembly to the bottom of the chassis.
   e. Remove the three T-15 Torx-drive screws securing the A09 Main Protocol assembly to the bottom of the chassis, and lift out the A09 Main Protocol assembly to complete its removal.
4. To reinstall the A09 Main Protocol assembly, perform steps 3a–3e in reverse order.

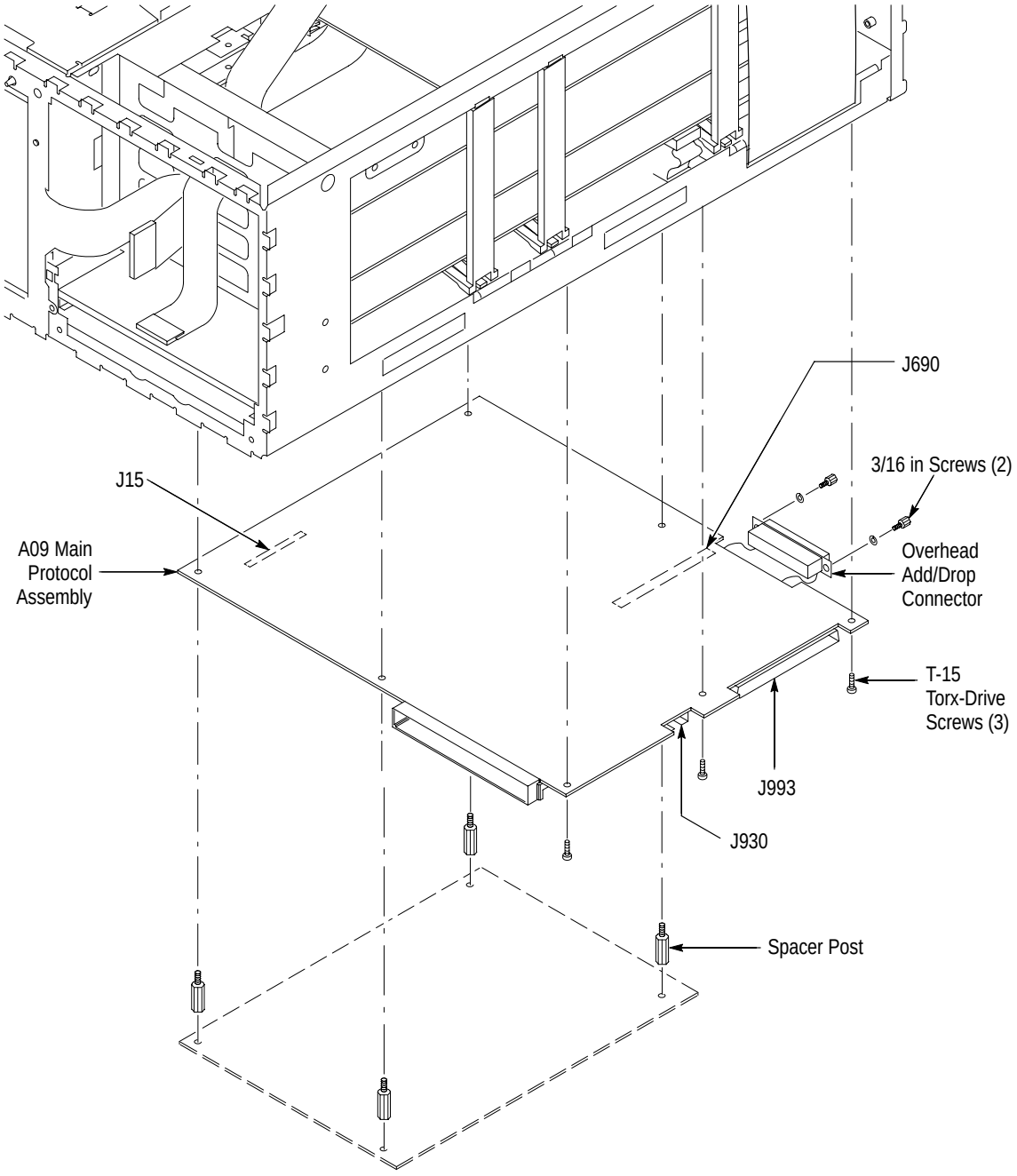


Figure 6–21: A09 Main Protocol Assembly Removal

A26 Monitor Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

NOTE. *The display tube and the display-driver board are a single module and must be removed and replaced as one unit. They are listed as a single module in the* Mechanical Parts List.

2. Set the CTS so its bottom is down on the work surface, with its front facing you.

WARNING. *Use care when handling a monitor. If you break its display tube it may implode, scattering glass fragments with high velocity and possibly injuring you. Wear protective clothing, including safety glasses (preferably a full-face shield). Avoid striking the display tube with or against any object.*

Store the monitor with its display tube face down in a protected location, placing it on a soft, nonabrasive surface to prevent scratching the face plate.

3. To remove the monitor, perform the following steps using Figure 6–22 as a guide:

a. Unplug the main cable at (J901), and then rotate the CTS so its top is down on the work surface, with its bottom facing upwards.

b. Remove the three T-15 Torx-drive screws securing the monitor assembly to the bottom of the main chassis. Return the CTS to the orientation established in step 2.

WARNING. *High voltage is present on the anode lead. It is not necessary to unplug the anode from the monitor when removing or replacing the monitor module; therefore, do not do so.*

c. Remove the three T-15 Torx-drive screws securing the monitor assembly to the top of the chassis. (See Figure 6–22 to locate the screws.)

d. Lift the left top flex lock on the trim ring, and pull the left corner of the trim ring forward slightly. (The left top flex lock is shown in Figure 6–14 on page 6–31.)

e. Tilt the rear of the monitor assembly upward slightly. Slide the monitor assembly back in the main chassis until it stops (about 3/4 inch). Now lift it straight up out of the top of the main chassis to complete the removal.

f. Store the monitor assembly in a protected location. Place it face down on a soft, nonabrasive surface to prevent scratching the face plate.

g. If replacing the CRT filter frame, press the locking tab at the top center of the frame while pushing the frame into the CTS. Lift the frame out of the chassis to complete its removal.

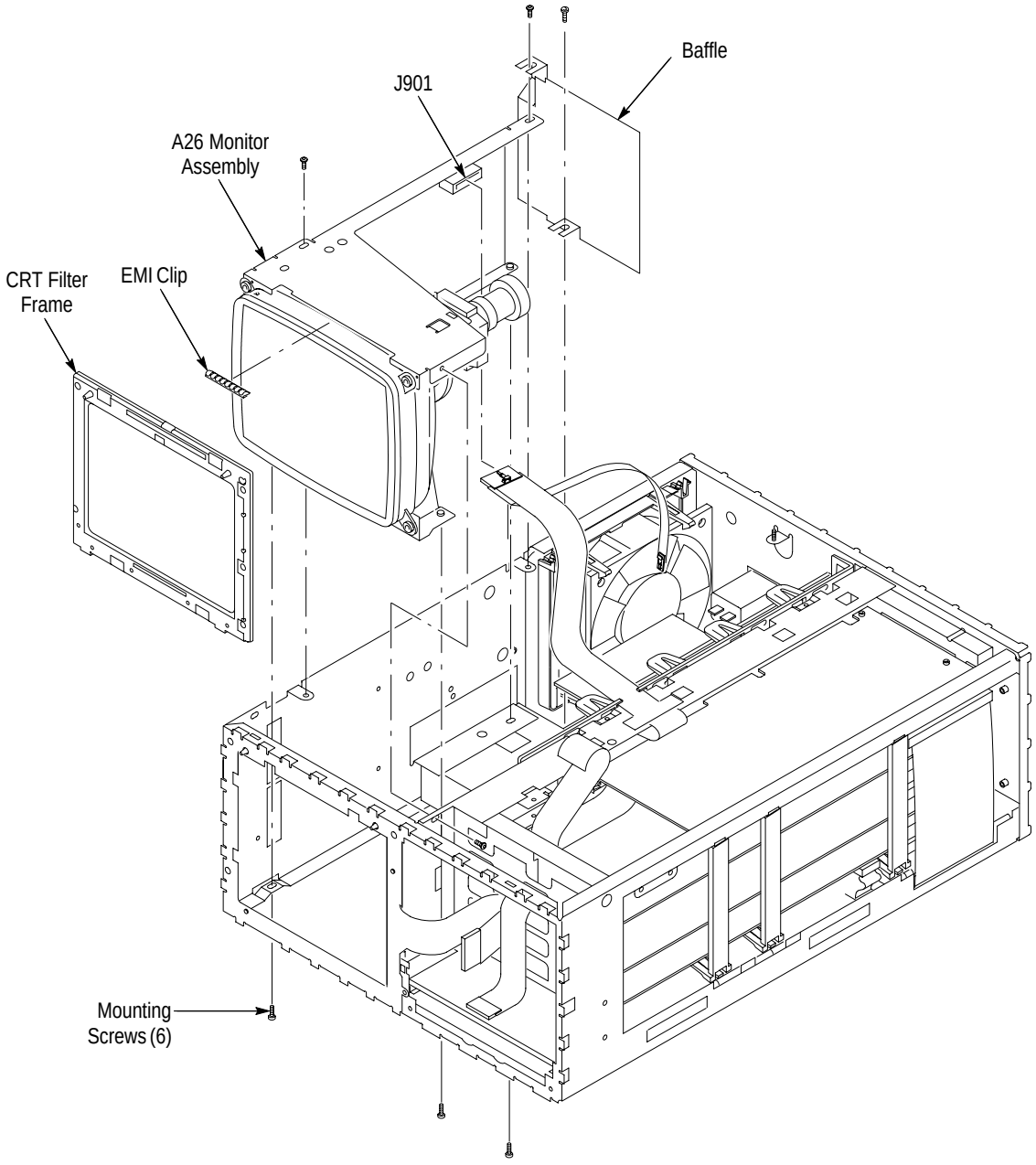


Figure 6–22: A26 Monitor Assembly Removal

4. To reinstall the filter frame and monitor, perform steps 3a–3g in reverse order. If the EMI clips on the monitor are replaced, be sure to center them in the notched area of the top and bottom of the chassis.

Com Bus, Board Supports, and PCAT Bus

For this procedure, no tools are required.

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. Press the snap lock at the bottom end of the board support and tilt the support outwards to remove from the chassis (see Figure 6–23). Repeat for the second and third board supports.

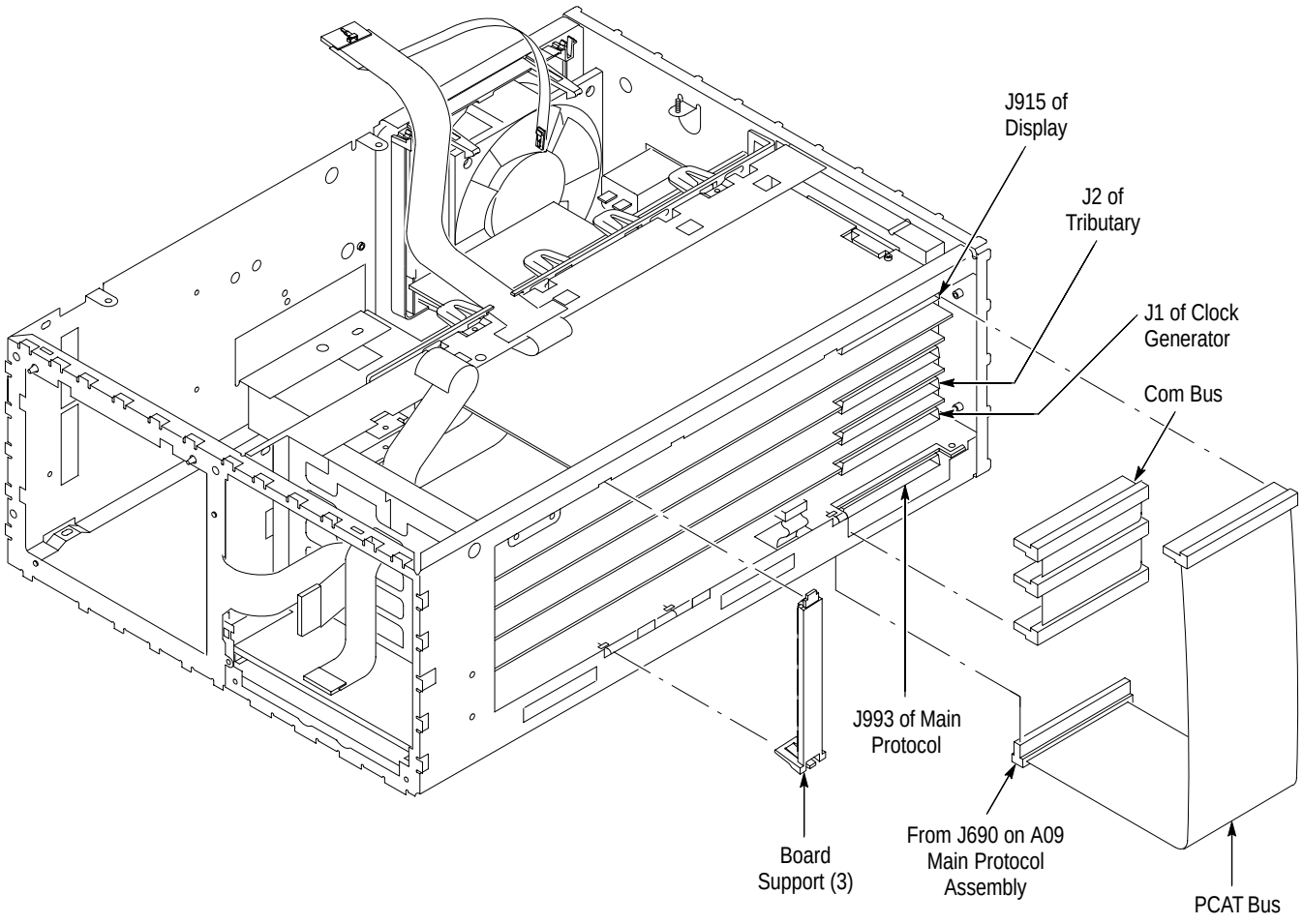


Figure 6–23: Com Bus, Board Supports, and PCAT Bus Removal

4. Grasp the PCAT bus by its cable pull tab and pull to unplug it from J915 of the Display assembly. Then grasp the connector and pull to unplug it from J690 of the A09 Main Protocol assembly (see Figure 6–23).

CAUTION. *Do not pull on the cable. Pulling on the cable will damage the cable or connector.*

5. Grasp the Com Bus connector, and pull to unplug it from J2 of the Tributary assembly and J1 of the A08 Clock Generator assembly. Then grasp the connector, and pull to unplug it from J993 of the A09 Main Protocol assembly (see Figure 6–23).

EMI Shield

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2) and a flat-bladed screwdriver (item 4).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down, with its back facing you.
3. To remove the EMI shield, perform the following steps using Figure 6–24 as a guide:
   a. Working from the rear of the CTS, remove the five T-15 Torx-drive screws that secure the EMI Shield to the rear of the chassis.
   b. Insert the flat-bladed screwdriver in the corners of the shield near the center of the rear panel. Gently pry the edge of the shield away from the chassis.
   c. Working from the rear of the CTS, grasp the shield and pull it away from the CTS to complete its removal.
4. To reinstall the EMI shield, perform steps 3a–3c in reverse order. Make certain the edge of the EMI shield slides under the screws securing the board assemblies.

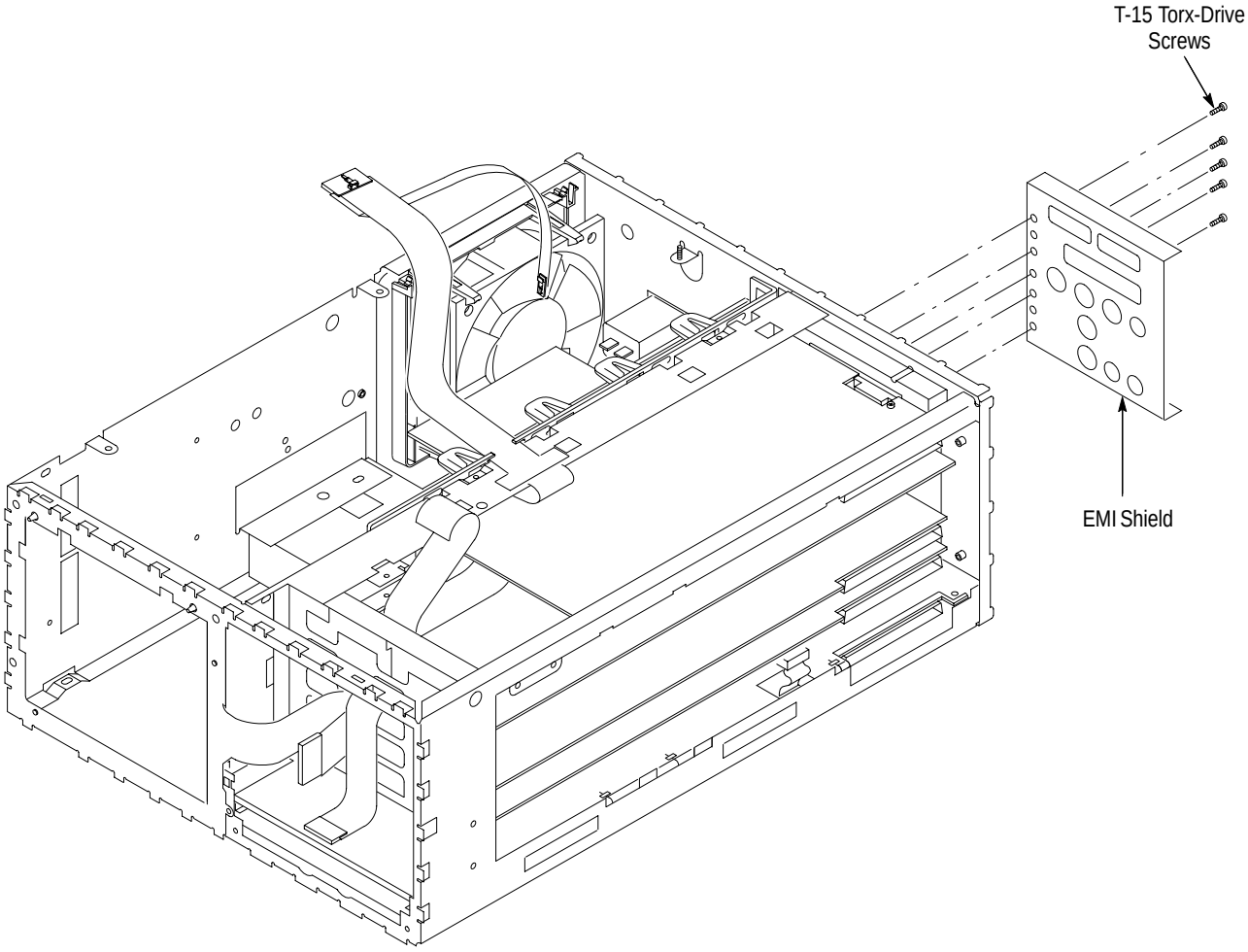


Figure 6–24: EMI Shield Removal

A03 CPU Assembly

When you disconnect the battery, you will lose all saved front panel setups. Adjustment constants, stored internally when the CTS is adjusted, are not lost.

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the CPU board, perform the following steps using Figure 6–25 as a guide:
   a. Remove the single T-15 Torx-drive screw from the bracket that secures the A03 CPU assembly at the inside rear corner of the main chassis.

b. Remove the cable from J3 of the A03 CPU assembly.

c. Grasp the board by its edge, and pull outward to unplug it from J2 of the backplane assembly.

d. Slide the board part way out until you can reach the CPU-to-front-panel cable at J4. Unplug the CPU-to-front-panel cable.

e. Slide the board part way out until you can reach the battery cable at J5. Unplug the battery cable.

f. Slide the board the rest of the way out of the main chassis to complete its removal.

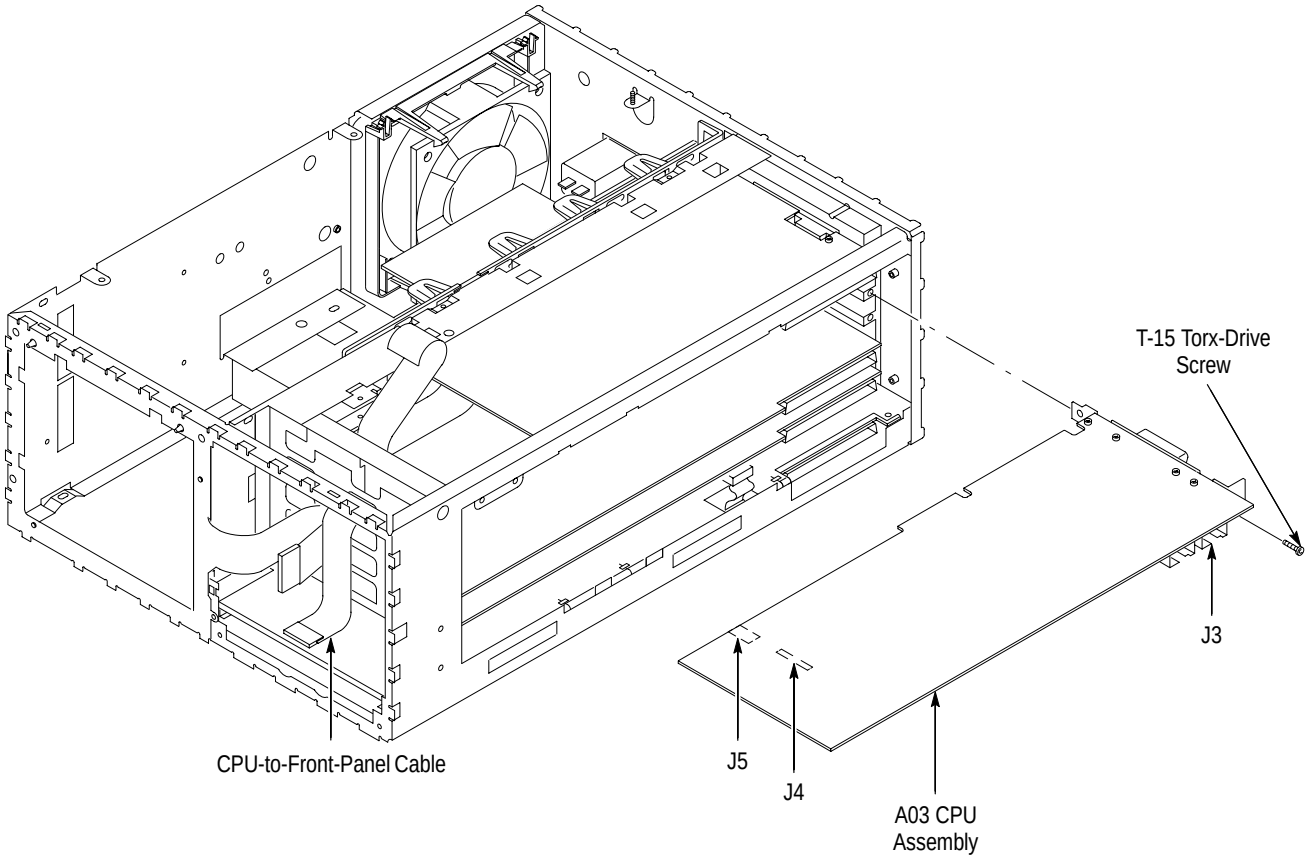


Figure 6–25: A03 CPU Removal

4. To reinstall the A03 CPU assembly, perform steps 3a–3f in reverse order. After plugging in the CPU-to-front-panel cable at J4, be sure to dress the cable so that the loop of extra cable is tucked behind the A06 Front Panel assembly, as shown in Figure 6–25. The cable should come from J4 on the CPU assembly and route directly through the chassis opening to the front-panel cavity.

A01 Display Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the A01 Display assembly, perform the following steps using Figure 6–26 as a guide:
   a. Unplug the monitor-to-display cable at J201.
   b. Lift up on the two locking tabs on J1 of the disk drive.
   c. Remove the cable from the disk drive.
   d. Remove the single T-15 Torx-drive screw from the bracket that secures the A01 Display assembly at the inside rear corner of the main chassis.
   e. Grasp the board by its edge, and pull outward to unplug it from J1 of the A02 Backplane assembly to complete the removal.
   f. Lift up on the two locking tabs on J60 of the A01 Display assembly. Remove the cable from the A01 Display assembly.
4. To reinstall the A01 Display assembly, perform steps 3a–3f in reverse order.

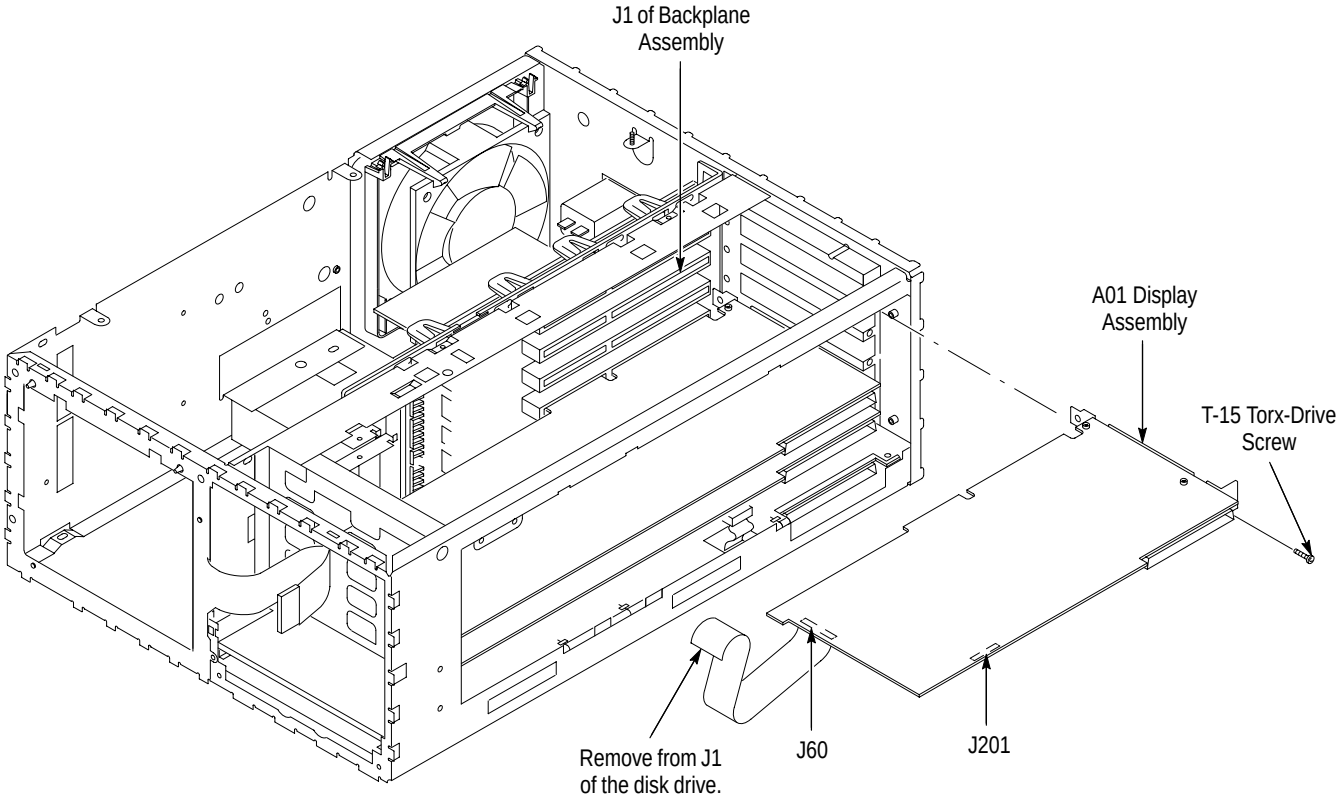


Figure 6–26: A01 Display Assembly Removal

A08 Clock Generator Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the A08 Clock Generator assembly, perform the following steps using Figure 6–27 as a guide:
   a. Unplug the Main Protocol-to-Clock Generator cable at J2 of the A08 Clock Generator assembly.
   b. Remove the single T-15 Torx-drive screw from the bracket that secures the A08 Clock Generator assembly at the inside rear corner of the main chassis.
   c. Grasp the board by its edge, and pull upward to unplug it from J5 of the backplane assembly.

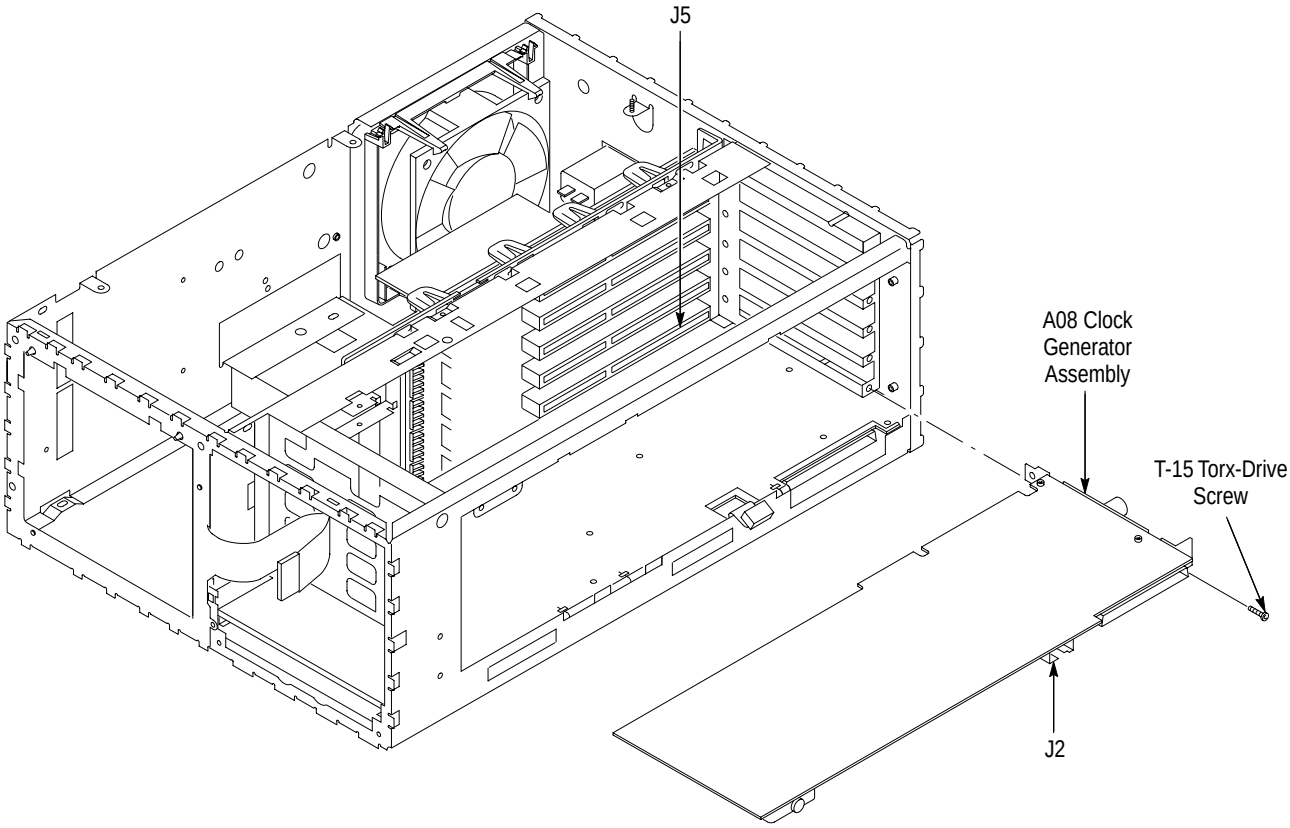


Figure 6–27: A08 Clock Generator Removal

d. As you remove the assembly, you will need to tilt it slightly so that the rear connectors can clear the chassis. Slide the assembly out of the chassis to complete the removal.

4. To reinstall the A08 Clock Generator assembly, perform steps 3a–3d in reverse order.

Tributary Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

2. Set the CTS so its left side is down, with its front facing to the left of you.

3. To remove the Tributary assembly, perform the following steps using Figure 6–28 as a guide:

   a. Unplug the Tributary-to-front- and rear-panel cables from the Tributary assembly (J225, J217, J218, and J220 on Option 22; J225, J5, J6, and J7 on Option 36).

   b. Remove the single T-15 Torx-drive screw from the bracket covering the center rear-panel slot at the inside rear corner of the main chassis.

   c. Remove the single T-15 Torx-drive screw from the bracket that secures the Tributary assembly at the inside rear corner of the main chassis.

   d. Grasp the board by its edges, and pull upward to unplug it from the backplane assembly.

   e. Slide the board the rest of the way out of the main chassis to complete its removal.

4. To reinstall the Tributary assembly, perform steps 3a–3e in reverse order.

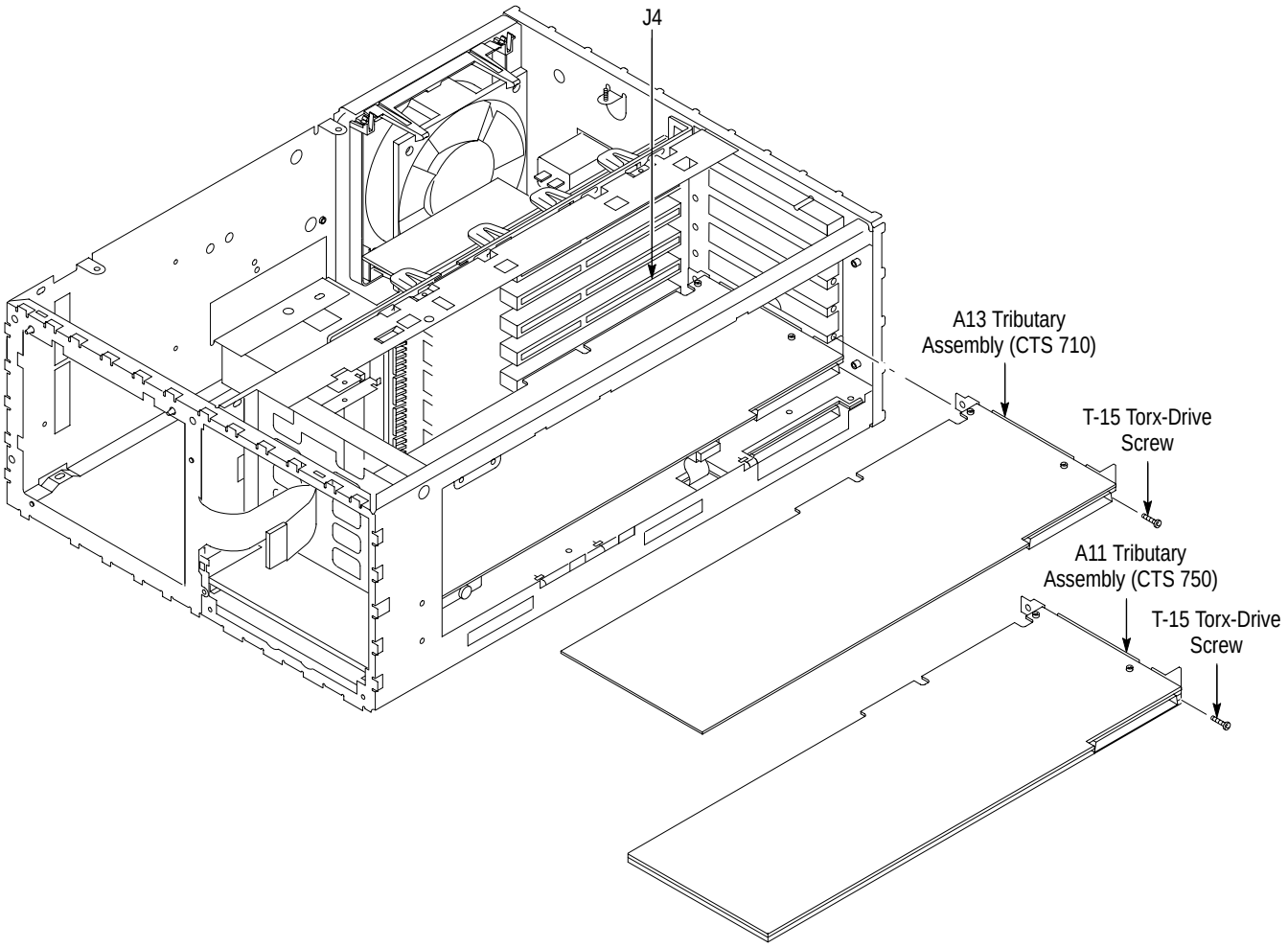


Figure 6–28: Tributary Removal

JAWA/JAWG Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the JAWA/JAWG assembly, perform the following steps using Figure 6–29 as a guide:
   a. Unplug the cables to the JAWA/JAWG assembly (J130, J140, J142, J150, J230, J240, J260, and J270).
   b. Remove the single T-15 Torx-drive screw from the bracket covering the center rear-panel slot at the inside rear corner of the main chassis.

c. Remove the single T-15 Torx-drive screw from the bracket that secures the JAWA/JAWG assembly at the inside rear corner of the main chassis.

d. Grasp the board by its edges, and pull upward to unplug it from the backplane assembly.

e. Slide the board the rest of the way out of the main chassis to complete its removal.

4. To reinstall the JAWA/JAWG assembly, perform steps 3a–3e in reverse order.

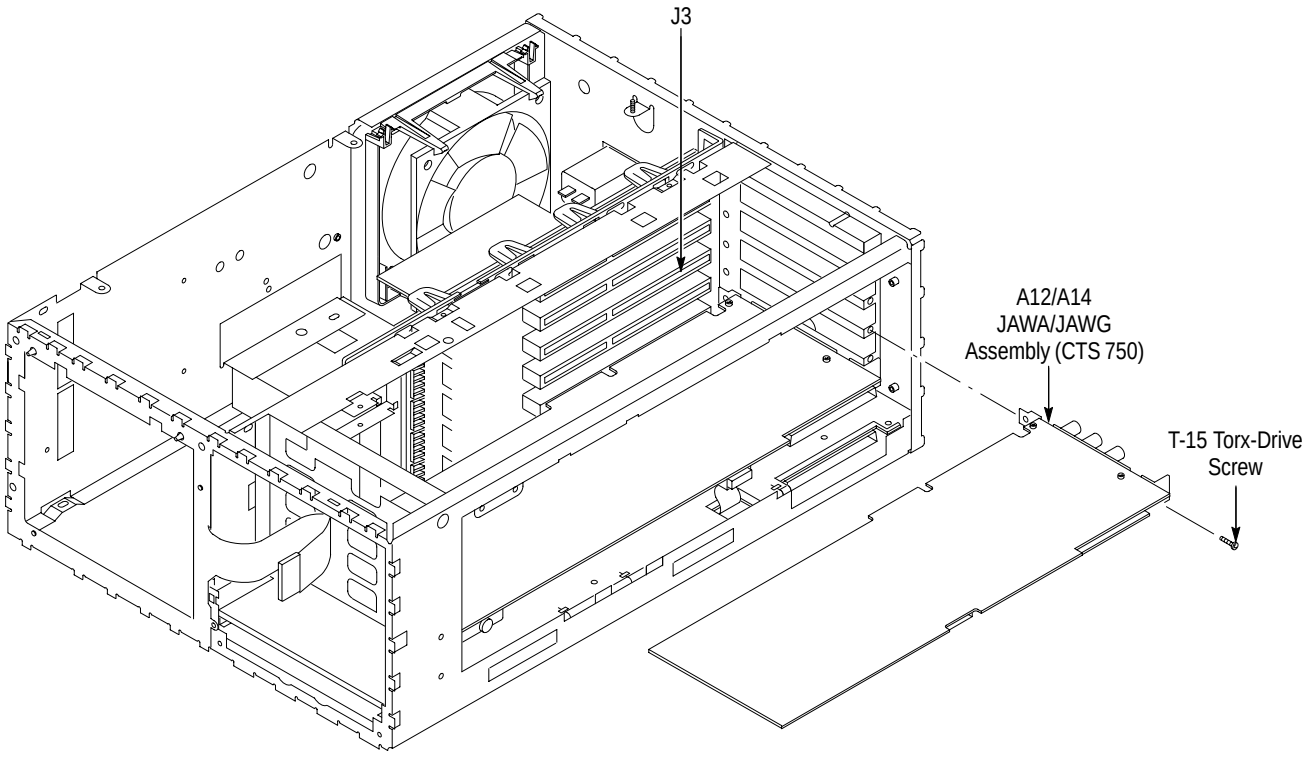


Figure 6–29: JAWA/JAWG Removal

A02 Backplane Assembly

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2) and a flat-bladed screwdriver (item 4).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left.
3. To remove the A02 Backplane assembly, perform the following steps using Figure 6–30 as a guide:
   - **a.** Remove any unused board brackets, mounted on the rear panel, that correspond to unused board slots in the backplane assembly. To remove the bracket, remove the single T-15 Torx-drive screw that secures the bracket at the inside rear corner of the main chassis.
   - **b.** Unplug the Backplane-to-Low Voltage Power Supply-to-Main Protocol cable at J7 of the A02 Backplane assembly.
   - **c.** Unplug the Backplane-to-AUX power cable at J6 of the A02 Backplane assembly.
   - **d.** Remove the five T15 Torx-drive screws mounting the board to the chassis.
   - **e.** Turn the CTS so its bottom is facing down on the work surface. Leave its front facing to the left.
   - **f.** Find the flex lock nearest the front of the CTS (shown in Figure 6–30). Using a flat-bladed screwdriver, push the flex lock so it flexes enough to clear the board.
   - **g.** While holding the flex lock, slightly pull up on the front corner of the board nearest that retainer until it clears that flex lock. Repeat for the remaining three flex locks.
   - **h.** Once the board is clear of all four flex locks, grasp the board by the edge near those flex locks, rotate that edge upwards slightly, and pull the board out of its retainer slot at its opposite edge.
   - **i.** Lift the assembly all of the way out of the chassis to complete the removal.
4. To reinstall the A02 Backplane assembly, perform steps 3a–3i in reverse order. Be sure to align the board to the retainer slot when doing step 3h. Seat the board until the four retainers snap over the edge of the backplane assembly when doing step 3g.

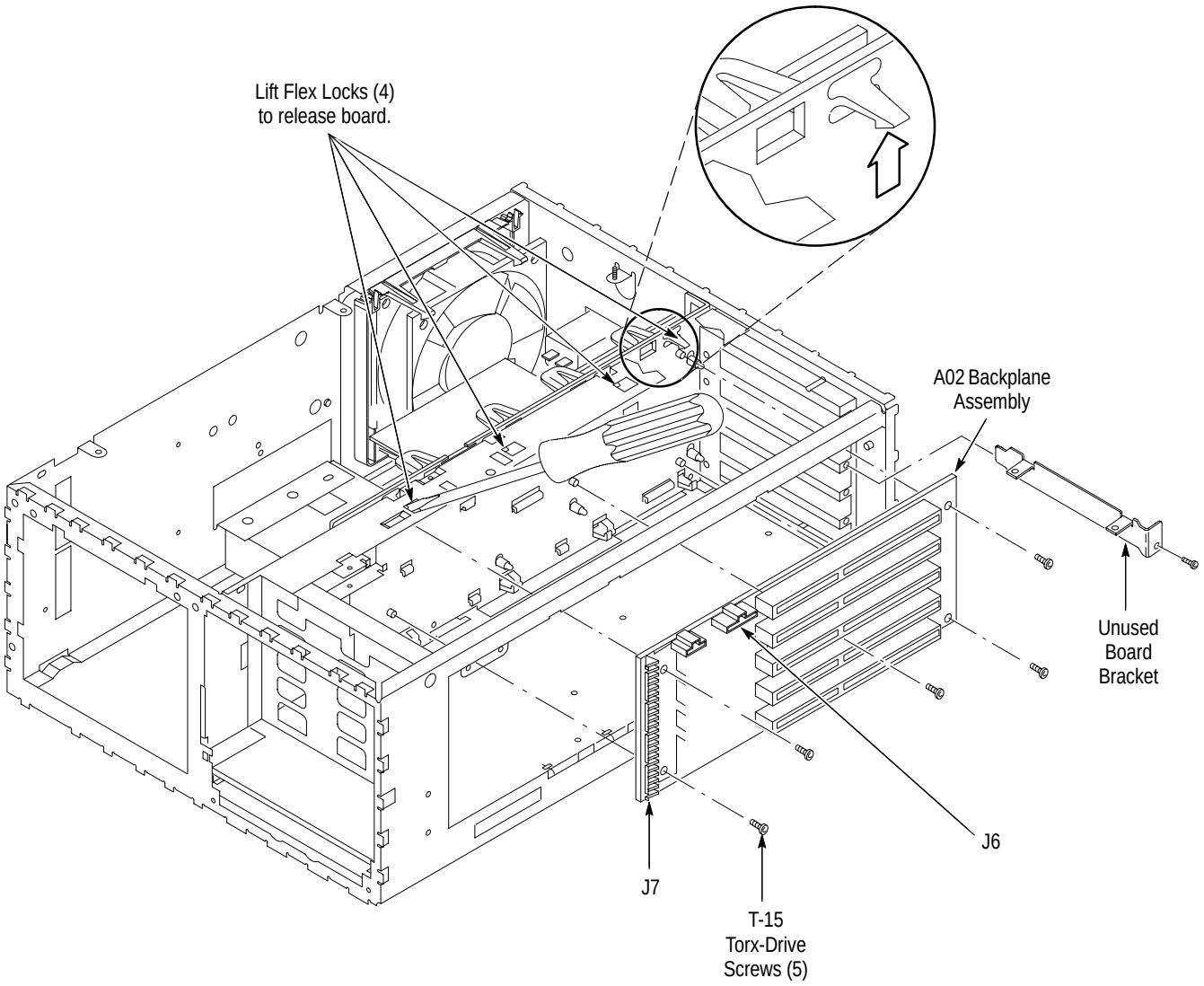


Figure 6–30: A02 Backplane Assembly

Back-Up Battery

When you disconnect the battery, you will lose all saved front panel setups. Adjustment constants, stored internally when the CTS is adjusted, are not lost.

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

WARNING. *The battery used in this CTS can present a fire or chemical burn hazard if mistreated. Do not recharge, rapidly discharge, disassemble, heat above 100° C, or incinerate.*

Replace the battery with the part number listed in the Mechanical Parts List *section only. Use of another battery may present a risk of fire or explosion.*

Dispose of used batteries promptly. Small quantities of used batteries may be disposed of in normal refuse. Keep away from children. Do not disassemble and do not dispose of in fire.

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its top is down on the work surface, with its right side facing you.
3. To remove the back-up battery, pull the battery out of its clamp near the front of the chassis (see Figure 6–31).
4. If removing the battery retainer, remove the T-15 Torx-drive screw from the battery retainer. Lift the battery retainer out of the chassis to complete its removal.

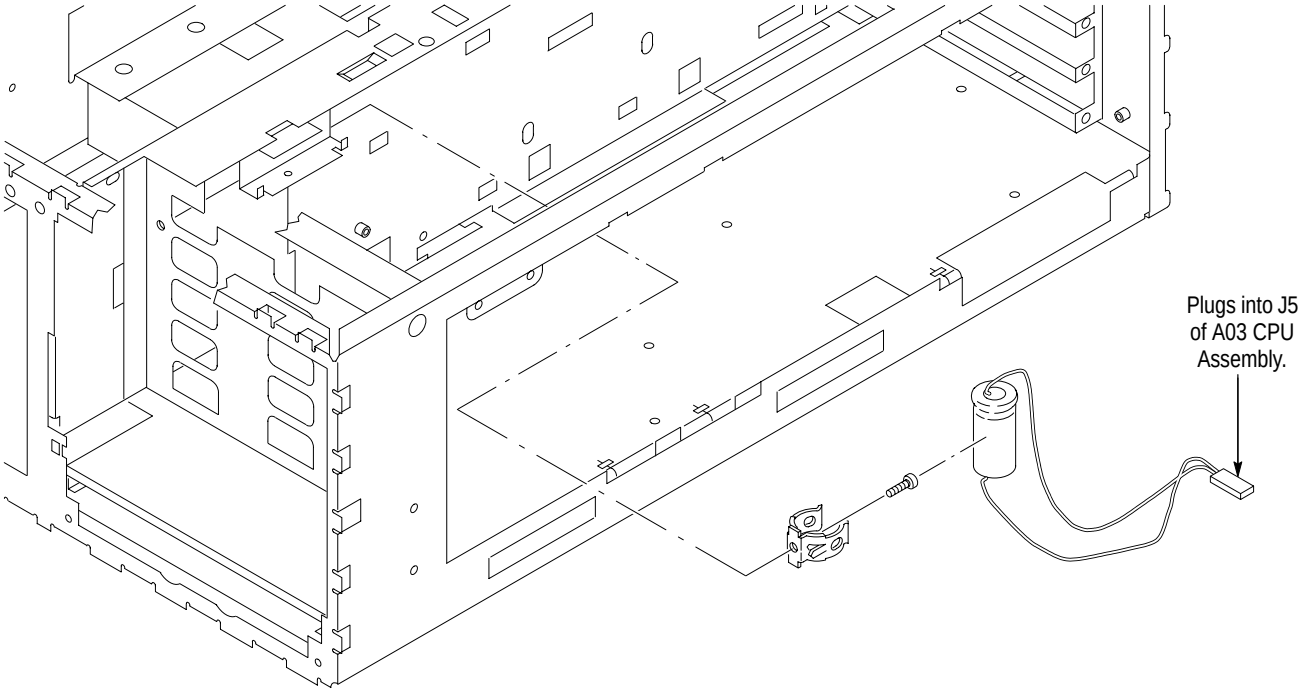


Figure 6–31: Battery Removal

5. To reinstall the battery and its retainer, perform steps 2 and 3 in reverse order.

Fan and Fan Mount

For this procedure, no tools are required.

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down, with its rear facing you.
3. To remove the fan, perform the following steps using Figure 6–32 as a guide:
   a. Unplug the fan power cable from J3 on the Auxiliary Power Supply.
   b. Release the two flex locks securing the top of the fan to the fan mount (shown in Figure 6–32); then lift the fan out from the top of the chassis.

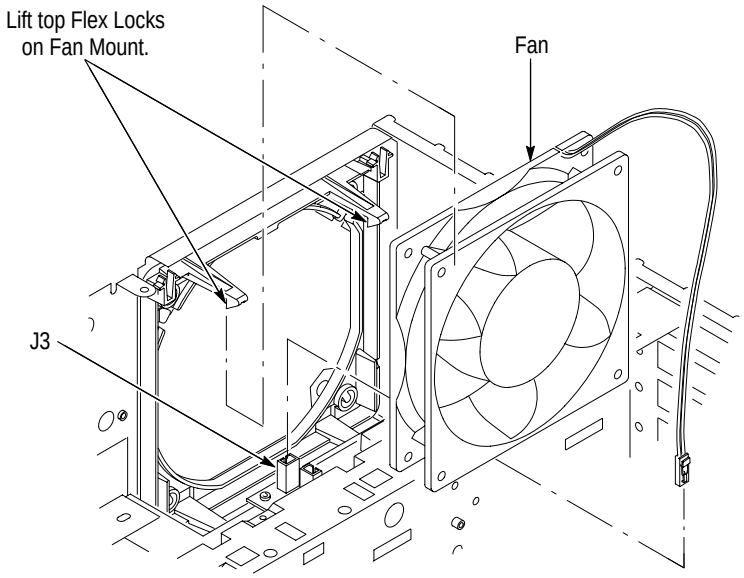


Figure 6–32: Fan Removal

***NOTE**. Do not do step 4 unless servicing a broken fan mount or removing the mount for cleaning.*

4. To remove the fan mount, perform the following steps using Figure 6–33 as a guide:
   a. Rotate the CTS so the side that houses the fan mount is facing upwards.
   b. Press the two flex locks to release them (see Figure 6–33).

c. While holding the flex locks released, slide the fan mount so its four retainer lugs slide from their small retainer holes in the chassis into their large release holes.

d. Move the fan mount inward so its retainer lugs are out of the large retainer holes, and lift it out of the chassis to remove.

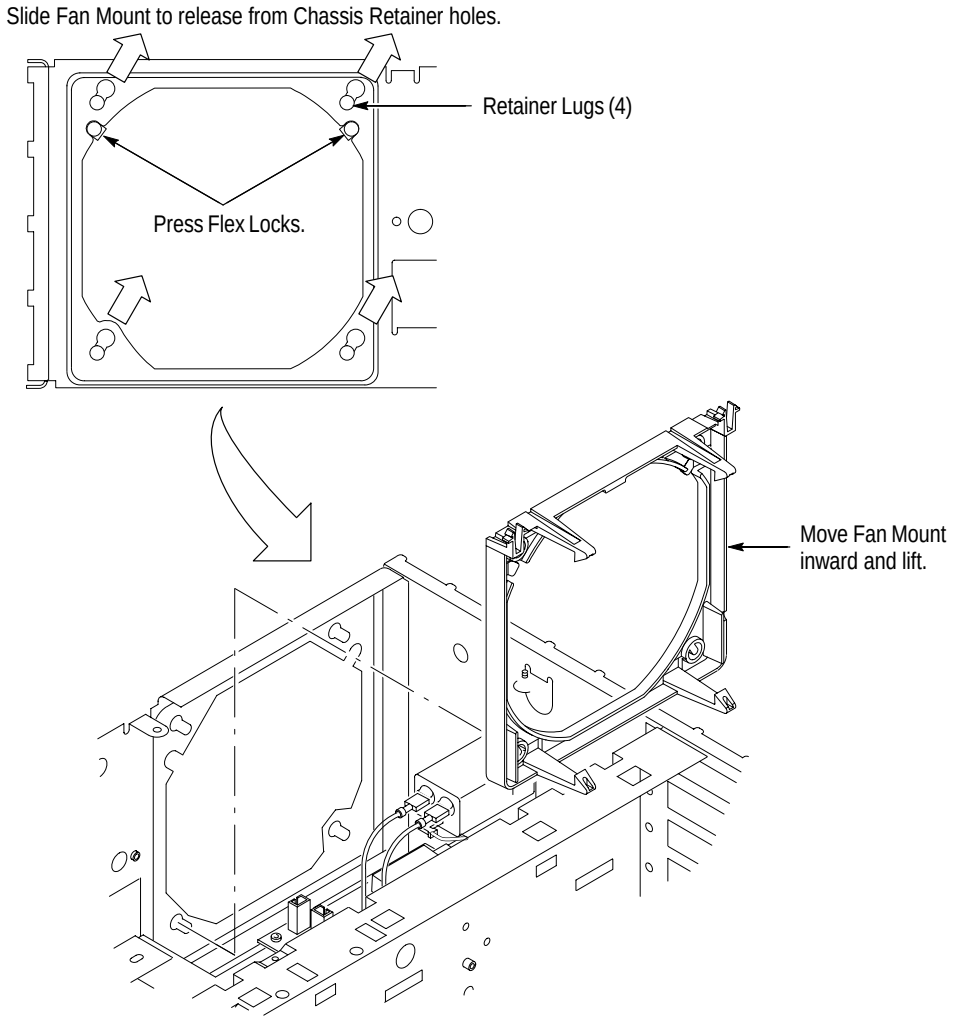


Figure 6–33: Fan Mount Removal

5. To reinstall the fan and its mount, perform the following steps:

a. If the fan mount was removed, perform steps 4a–4d in reverse order. Be sure to seat the fan mount so its two flex locks snap to secure it on the chassis.

b. To reinstall the fan, perform steps 3a–3b in reverse order. Be sure the two locks snap into place to secure the fan.

A25 Low Voltage Power Supply and its Mount

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2) and a pair of duck-bill pliers (item 6).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down on the work surface, with its front facing to the right.

CAUTION. *When releasing the Low Voltage Power Supply from its mount, take care not to push on the board components. Rather, push on the board edge when performing the following steps.*

3. To remove the Low Voltage Power Supply, perform the following steps using Figure 6–34 as a guide:

a. Unplug the cable coming from the backplane assembly at J2.

b. Unplug the cable coming from the AUX power supply at J1.

c. Unplug the AUX power cable at J7 on the A07 Auxiliary Power supply.

d. Unplug the monitor cable at J4 on the A07 Auxiliary Power supply.

e. Now, release and disconnect the remote-power cable where it joins the cable from the Low Voltage Power Supply assembly.

f. Working through the opening created when the fan was removed, remove the T-15 Torx-drive screw at the center of the power supply board.

g. Using a pair of duck-bill pliers, squeeze to release each of the four flex locks at the top edge of the Low Voltage Power Supply assembly.

h. Once released, tilt the board out away from the flex locks, and then unplug the AC power cable (remote power switch) where it connects to the cable from the Low Voltage Power Supply (J4).

i. Lift the Low Voltage Power Supply assembly out of the chassis to complete its removal.

NOTE*. Do not do step 4 unless servicing a broken power supply mount or removing the mount for cleaning.*

4. To remove the power-supply mount, perform the following steps:

   a. Place the CTS so its left side is down, with its top facing you.

   b. Press the two retainer locks, and slide the power-supply mount towards the top of the CTS to unlock from the chassis.

   c. Lift the power-supply mount out of the chassis to complete the removal.

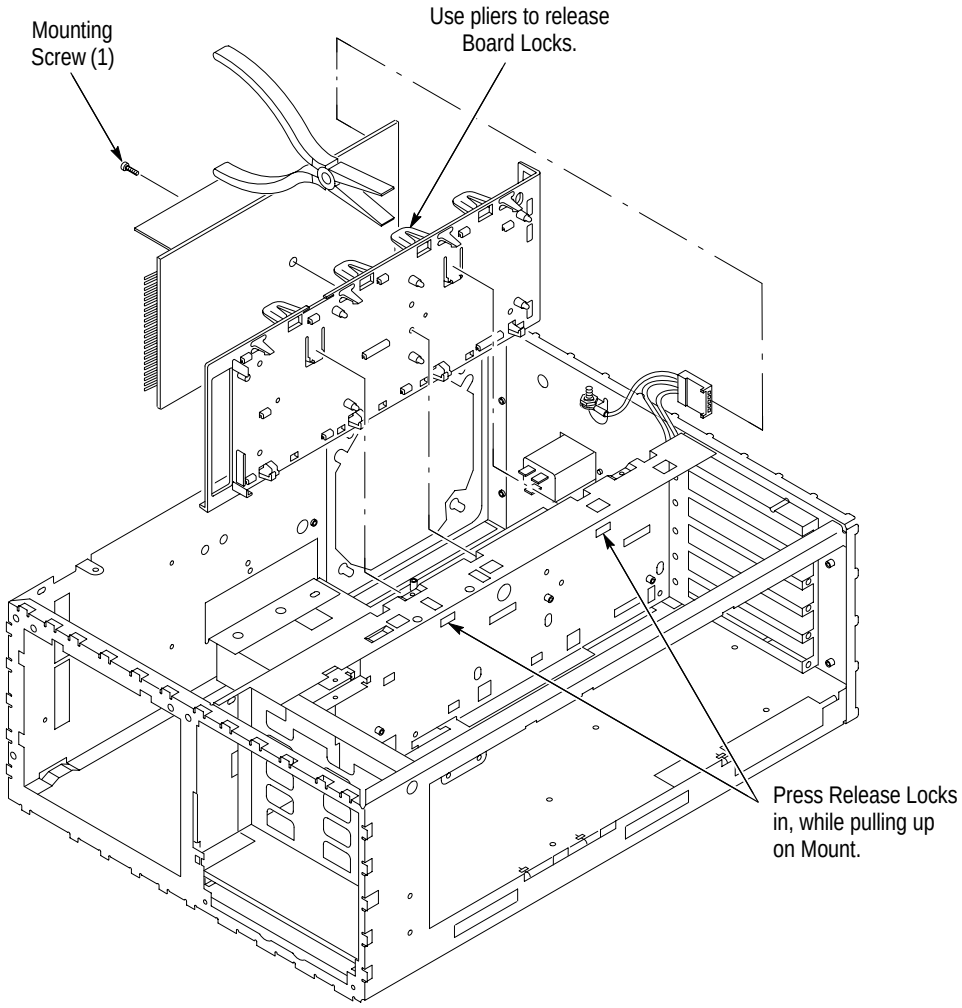


Figure 6–34: A25 Low Voltage Power Supply Removal

5. To reinstall the Low Voltage Power Supply and its mount, perform the following steps:

   a. If the power supply mount was removed, perform steps 4a–4c in reverse order. When reinstalling the power-supply mount, be sure to press it flush against the chassis before sliding it towards the bottom of the chassis to lock.

   b. To reinstall the Low Voltage Power Supply, perform steps 3a–3i in reverse order. Be sure to seat the board until all four flex locks are locked.

A07 Auxiliary Power Supply

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down on the work surface, with its rear facing you.

3. To remove the Auxiliary Power Supply, perform the following steps using Figure 6–35 as a guide:

   a. Unplug the monitor power cable at J4, the fan power cable at J3, the cable from the backplane assembly at J7, and the Low Voltage Power Supply cable at J1 on the Low Voltage Power Supply assembly.

   b. Release and disconnect the remote-power cable where it joins the cable from the Low Voltage Power Supply assembly.

   c. Unplug the two connectors at the line filter.

   d. Remove the two T-15 Torx-drive screws mounting the Auxiliary Power Supply to the chassis. Then pull up on the board to release it from the two retainers. Lift the board out of the chassis to complete the removal.

WARNING. *When reconnecting the Auxiliary Power Supply to the line filter, be sure to connect the neutral side of the line filter to the white-striped lead and the load side to the black-striped lead.*

4. To reinstall the Auxiliary Power Supply, perform steps 3a–3d in reverse order. Be sure to seat the board until the two mounting posts snap lock on the assembly when reinstalling. When finished, reverify that the wires to the line filter are connected correctly.

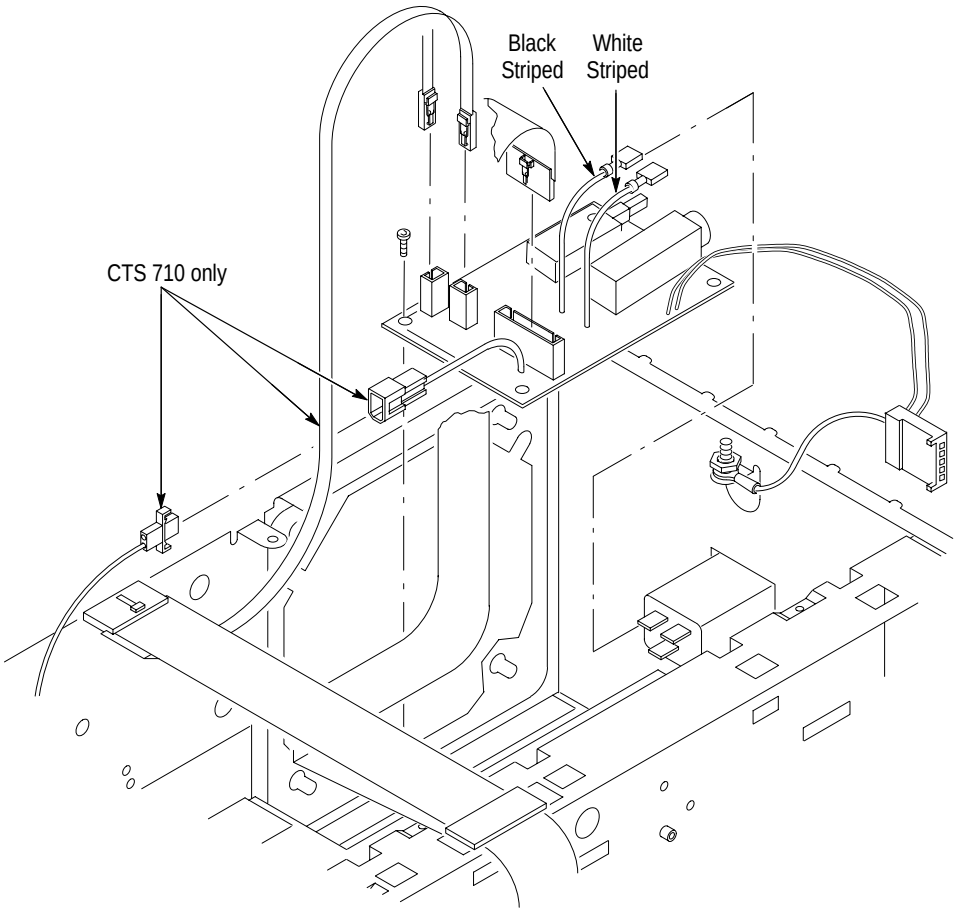


Figure 6–35: Auxiliary Power Supply Removal

Line Filter

For this procedure you will need a screwdriver with a size T-15 Torx tip (items 1 and 2).

1. If you have not already performed the *Access Procedure* on page 6–11 and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down on the work surface, with its rear facing you.
3. To remove the line filter, perform the following steps using Figure 6–36 as a guide:
   a. Unplug the three connectors at the line filter.
   b. Remove the two screws mounting the line filter to the chassis. Pull the filter out through the rear of the chassis to complete the removal.

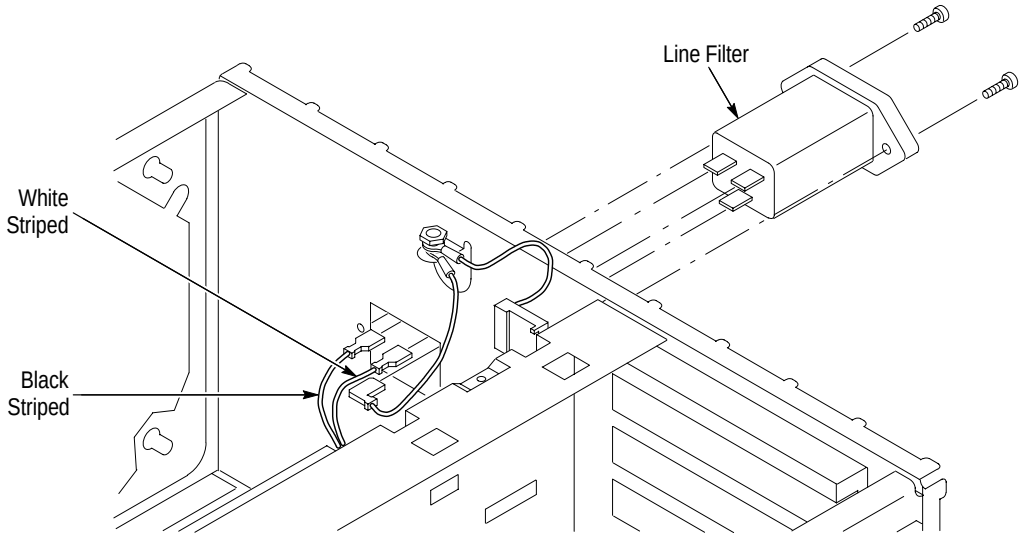


Figure 6–36: Line Filter Removal

WARNING. *When reconnecting the Auxiliary Power Supply to the line filter, be sure to connect the neutral side of the line filter to the white-striped lead and the load side to the black-striped lead.*

It is not necessary to disconnect the earth ground from the chassis lug that it is bolted to. If, however, you have done so, be sure to install the earth lead (and its nut) from the line filter before installing the earth lead (and its nut) from the Low Voltage Power Supply.

4. To reinstall the line filter, perform steps 3a–3b in reverse order. When finished, reverify that the wires from the Auxiliary Power Supply assembly are connected correctly.

Main Chassis

Since the removal of the main chassis requires the removal of virtually all modules, perform the procedure *Disassembly for Cleaning* that follows. To reinstall the main chassis, see reinstallation instructions in *Disassembly for Cleaning.*

Disassembly for Cleaning

This procedure is for disassembly of the CTS 700-Series Test Set into its individual modules so they can be cleaned. Read the cleaning instructions in *Inspection and Cleaning* on page 6–3 of this section before disassembling the CTS.

For this procedure you will need a screwdriver with a T-15 Torx tip (items 1 and 2), a T-20 Torx tip (item 3), a flat-bladed screwdriver (item 4), a hex key screwdriver (item 12), duck-bill pliers (item 6), spudger (item 13), a Pozidriv screwdriver (item 7), and a soldering iron (item 15).

1. Familiarize yourself with the modules illustrated in Figures 6–3, 6–4, and 6–5.
2. To completely disassemble the CTS, perform the following procedures in the order listed. They are found under *Procedures for Module Removal and Installation* which start on page 6–22.
   - **a.** *Line Fuse and Line Cord* (page 6–26)
   - **b.** *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet* (page 6–27)
   - **c.** *Plug-In Interface Module* (page 6–33)
   - **d.** *Disk Drive* (page 6–34)
   - **e.** *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets* (page 6–30)
   - **f.** *A06 Front Panel Assembly and Menu Flex Circuit* (page 6–35)
   - **g.** *Fan and Fan Mount* (page 6–58)
   - **h.** *A25 Low Voltage Power Supply and its Mount* (page 6–60)
   - **i.** *A26 Monitor Assembly* (page 6–42)
   - **j.** *A07 Auxiliary Power Supply* (page 6–62)
   - **k.** *Line Filter* (page 6–63)
   - **l.** *EMI Shield* (page 6–46)
   - **m.** *Com Bus, Board Supports, and PCAT Bus* (page 6–45)
   - **n.** *A08 Clock Generator Assembly* (page 6–50)
   - **o.** *Tributary Assembly* (page 6–51)
   - **p.** *A12/A14 JAWA/JAWG Assembly* (page 6–53)

q. *A03 CPU Assembly* (page 6–47)

r. *A01 Display Assembly* (page 6–49)

s. *A02 Backplane Assembly* (page 6–55)

t. *Back-Up Battery* (page 6–56)

u. *A10 High Speed Protocol Assembly* (page 6–39)

v. *A09 Main Protocol Assembly* (page 6–41)

3. To completely reassemble the CTS, perform the following procedures in the order listed. Observe these general instructions as you perform them:

- When doing the listed procedures, perform their steps in reverse order.
- When reinstalling the modules, ignore any instructions that require connecting a cable or bus to a module that you have not yet installed. You will make the necessary connections when you install the missing module.
- Ignore any instructions to do the *Access Procedure*. The access procedure is only used when removing individual modules for servicing, not when doing a disassembly/reassembly for cleaning.

a. *A09 Main Protocol Assembly* (page 6–41)

b. *A10 High Speed Protocol Assembly* (page 6–39)

c. *Line Filter* (page 6–63)

d. *A07 Auxiliary Power Supply* (page 6–62)

e. *A26 Monitor Assembly* (page 6–42)

f. *A25 Low Voltage Power Supply and its Mount* (page 6–60)

g. *Fan and Fan Mount* (page 6–58)

h. *Back-Up Battery* (page 6–56)

i. *A02 Backplane Assembly* (page 6–55)

j. *A01 Display Assembly* (page 6–49)

k. *A03 CPU Assembly* (page 6–47)

l. *A12/A14 JAWA/JAWG Assembly* (page 6–53)

m. *Tributary Assembly* (page 6–51)

n. *A08 Clock Generator Assembly* (page 6–50)

o. *EMI Shield* (page 6–46)

p. *Com Bus, Board Supports, and PCAT Bus* (page 6–45)

q. *A06 Front Panel Assembly and Menu Flex Circuit* (page 6–35)

r. *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets* (page 6–30)

s. *Disk Drive* (page 6–34)

t. *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet* (page 6–27)

u. *Line Fuse and Line Cord* (page 6–26)

Troubleshooting

This section contains information and procedures designed to help you isolate faulty modules in CTS 700-Series Test Sets. If a module needs to be replaced, follow the Removal and Replacement procedures beginning on page 6–9.

CAUTION. *The CTS operates over several ranges of line voltage (see* Power Requirements *on page 1–15 of* Specifications*). Before stepping the line voltage from one range to a higher range, set the principal power switch (rear panel) to its* ***OFF*** *position. Failure to do so can damage the CTS.*

Diagnostics

The CTS self-test diagnostics help you verify, adjust, and, if necessary, isolate faulty modules. The error reporting tells you which module is bad or leads you, with the help of the troubleshooting procedures, to the bad module.

The CTS has two levels of internal diagnostics, power-up and extended. At power-up the CTS automatically executes the power-up diagnostics and reports any bad modules or interfaces. The extended set is user selectable and tests CTS circuitry in-depth. It also reports any bad modules or interfaces.

Table 6–7 lists the modules tested by the diagnostics.

Table 6–7: Modules Tested by Power-Up and Extended Diagnostics

Module
A01 Display
A02 Backplane
A03 CPU
Plug-In Interface Module
A06 Front Panel
A07 Auxiliary Power
A08 Clock Generator
A09 Main Protocol
A10 High Speed Protocol
A25 Low Voltage Power Supply

Table 6–7: Modules Tested by Power-Up and Extended Diagnostics (Cont.)

Module
A11/A13 Tributary
A12/A14 JAWA/JAWG

Running Self Test

This procedure uses internal routines to verify that the CTS passes its internal self tests.

Equipment Required	No test equipment or connections are required
Prerequisites	Power up the CTS and allow a twenty minute warm-up period before running Self Test
Time Required	Approximately two minutes (after warm-up time)

Set up and execute the Self Test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys: Internal
		Self Test Control	Run

Refer to *Self Test* on page 4–14 and *System Self Test with External Loop-Back* on page 4–16 for more information about the extended diagnostics.

Troubleshooting Trees

Use this section in conjunction with the self test diagnostics to isolate a faulty module.

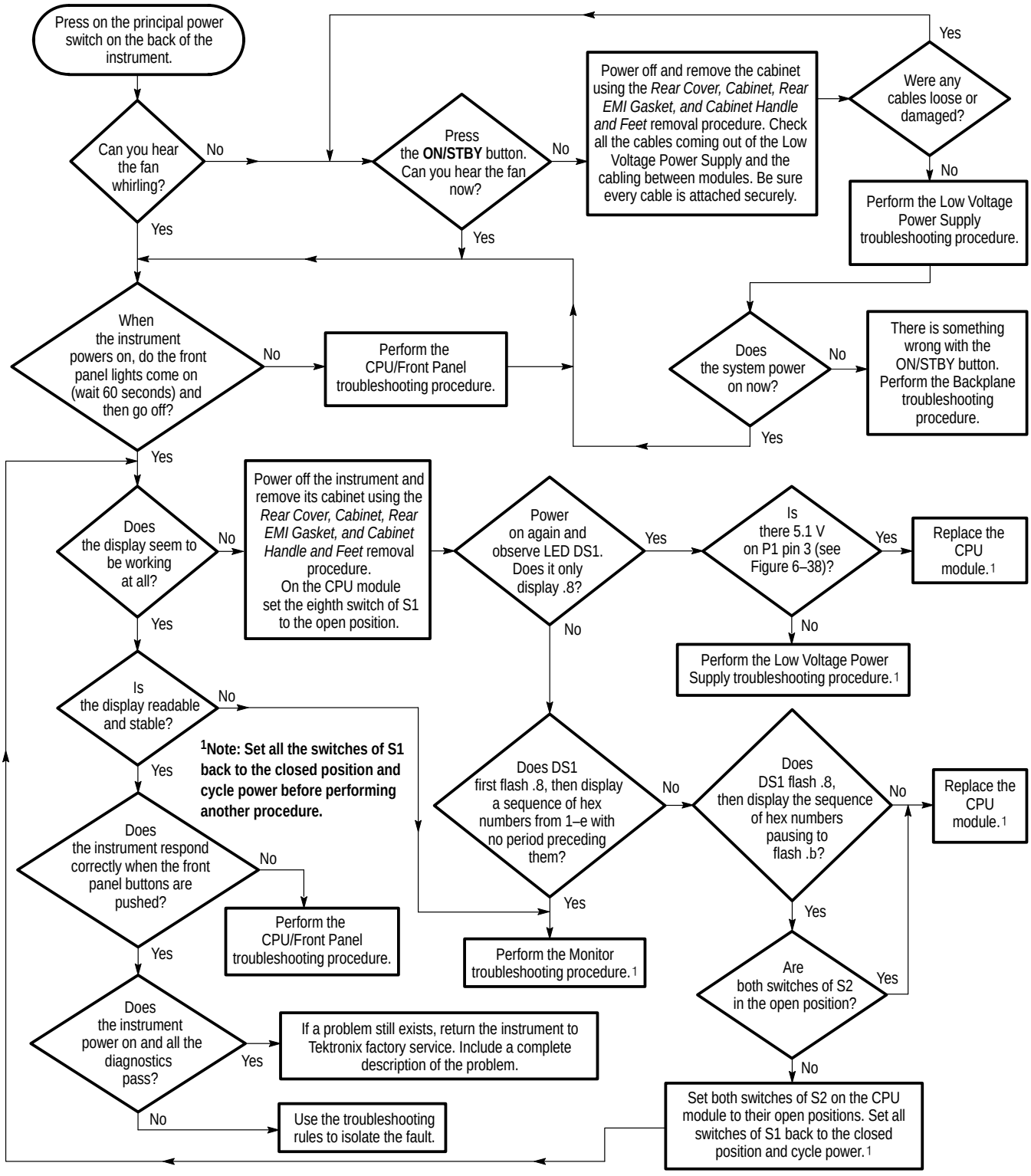


Figure 6–37: Primary Troubleshooting Procedure

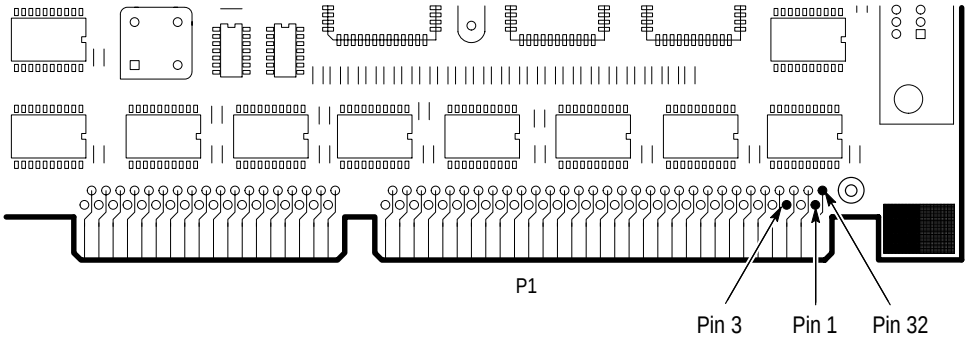


Figure 6–38: CPU Board Connector P1

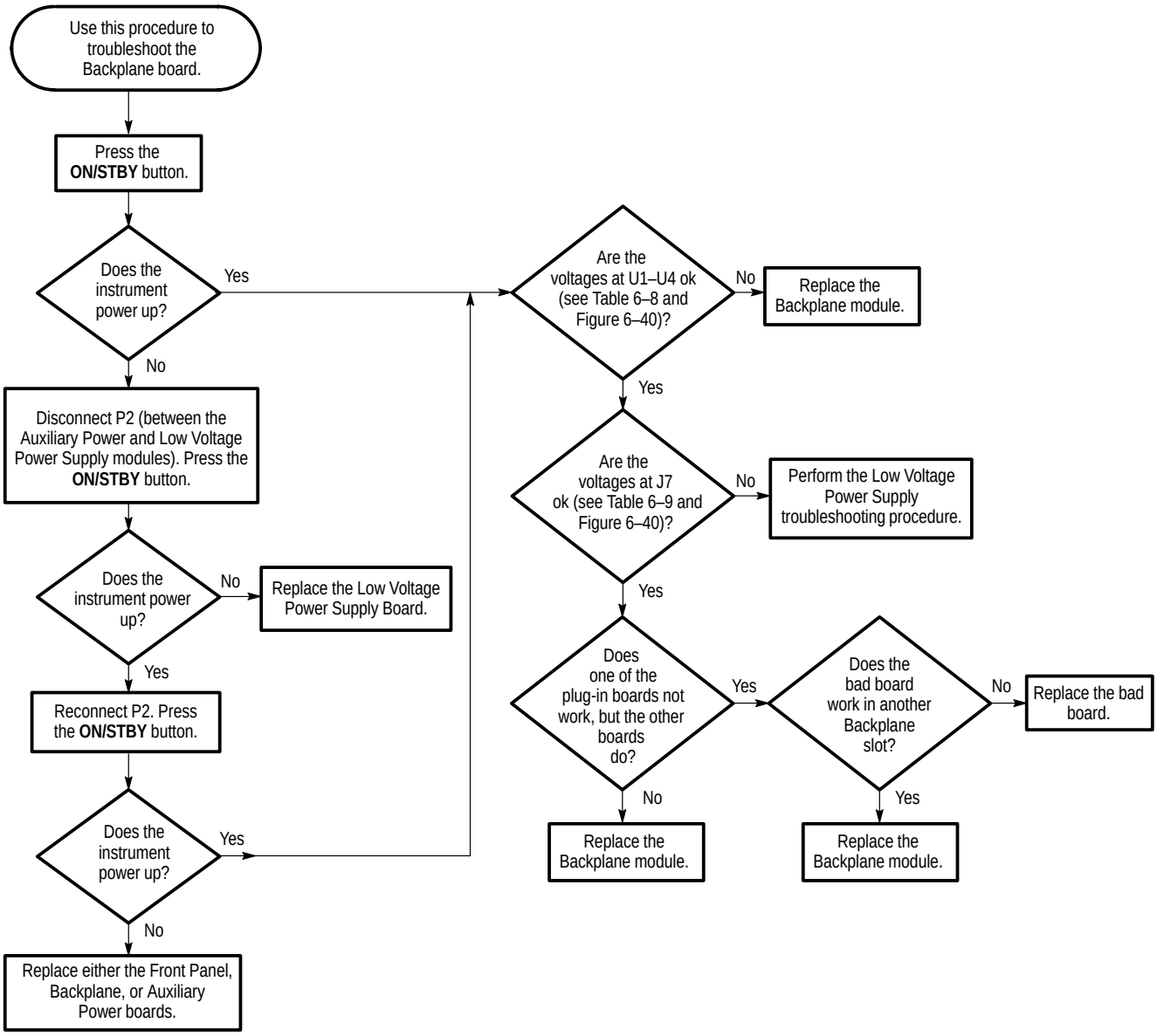


Figure 6–39: Backplane Troubleshooting Procedure

Table 6–8: Regulator Voltages

Regulator	Nominal Voltage	Minimum Voltage	Maximum Voltage
U1 pin 3	–12 V	–11.5 V	–12.5 V
U2 pin 3	+12 V	+11.5 V	+12.5 V
U4 pin 3	–6.4 V	–6.336 V	–6.464 V

Table 6–9: J7 Voltages

Pin	Nominal Voltage	Minimum Voltage	Maximum Voltage
1	–15 V	–14.85 V	–15.15 V
2	–15 V	–14.85 V	–15.15 V
7	–6.4 V	–6.336 V	–6.464 V
8	+15 V	+14.85 V	+15.15 V
9	+15 V	+14.85 V	+15.15 V
18	+5.1 V	+5.151 V	+5.05 V
19	+5.1 V	+5.151 V	+5.05 V

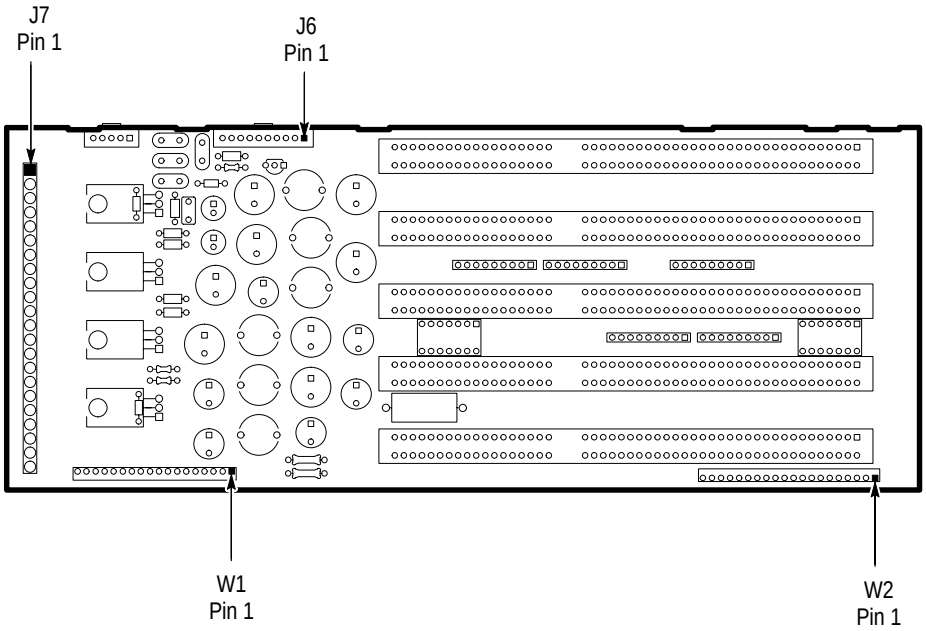


Figure 6–40: Backplane Module

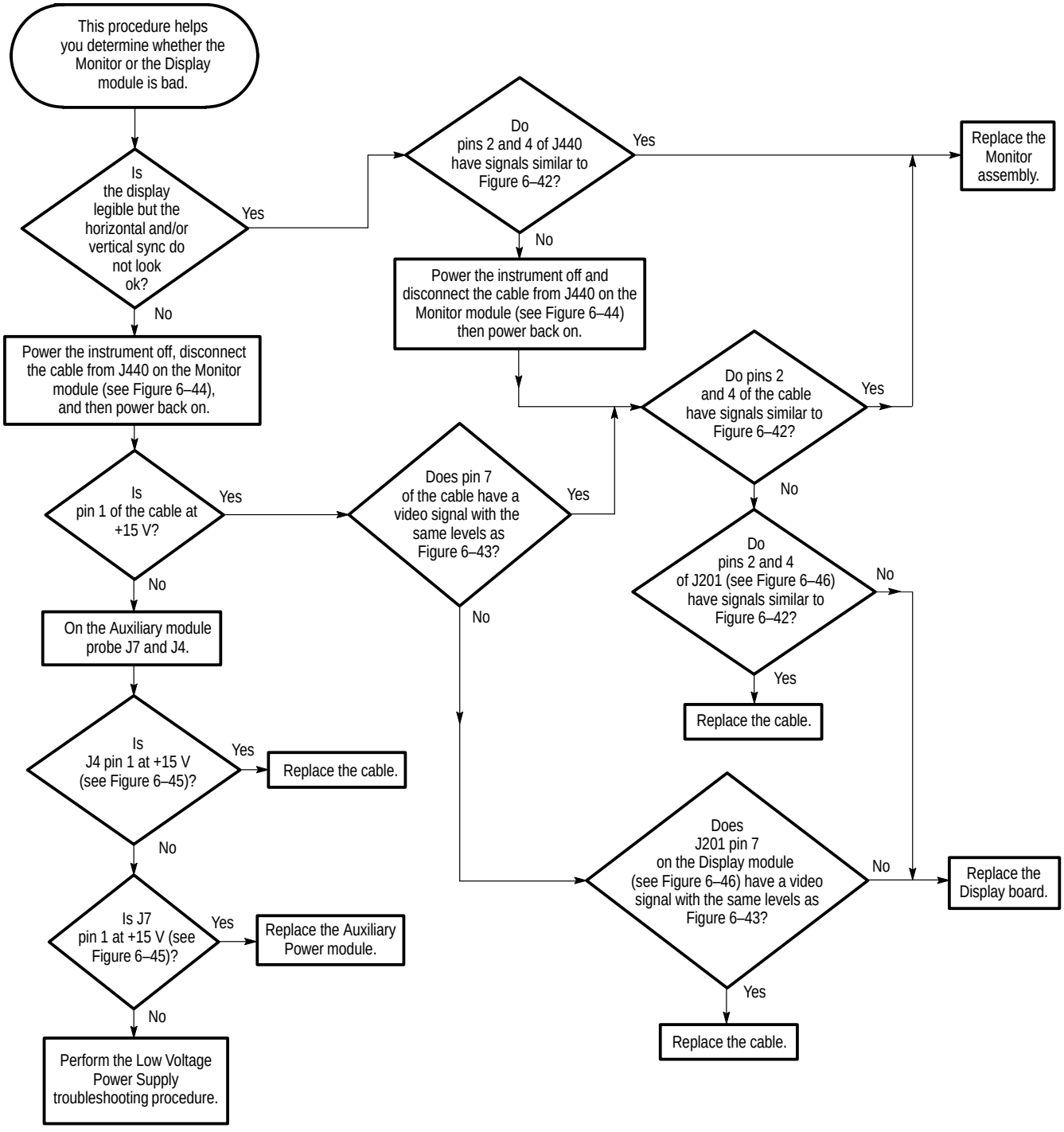


Figure 6–41: Monitor Troubleshooting Procedure

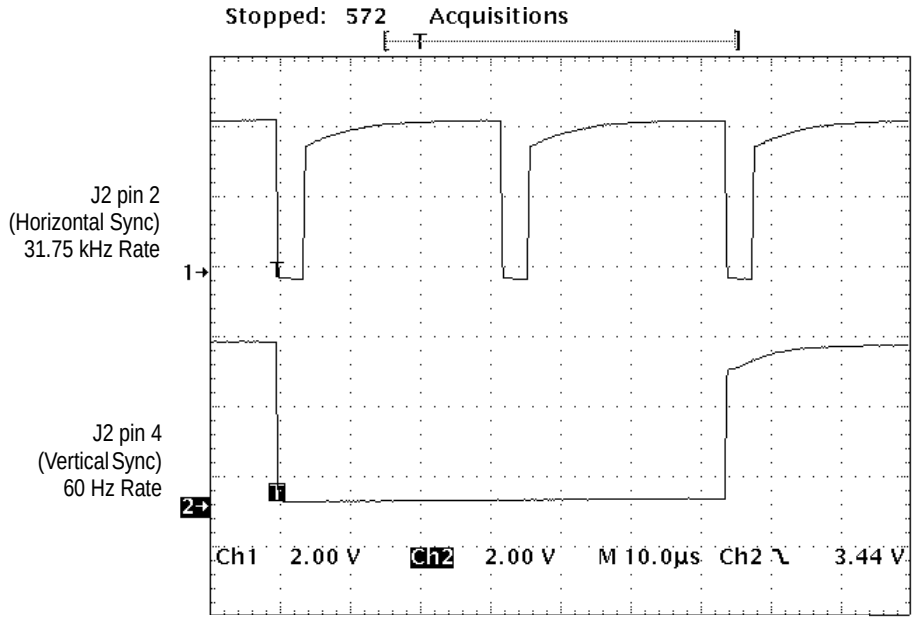


Figure 6–42: Horizontal and Vertical Sync Signals

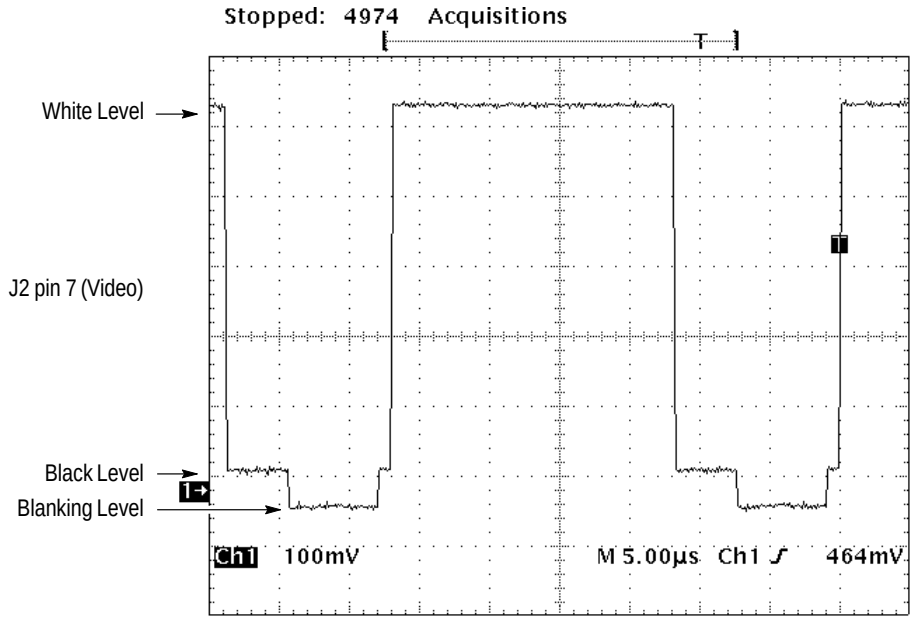


Figure 6–43: A Video Signal with White, Black, and Blanking

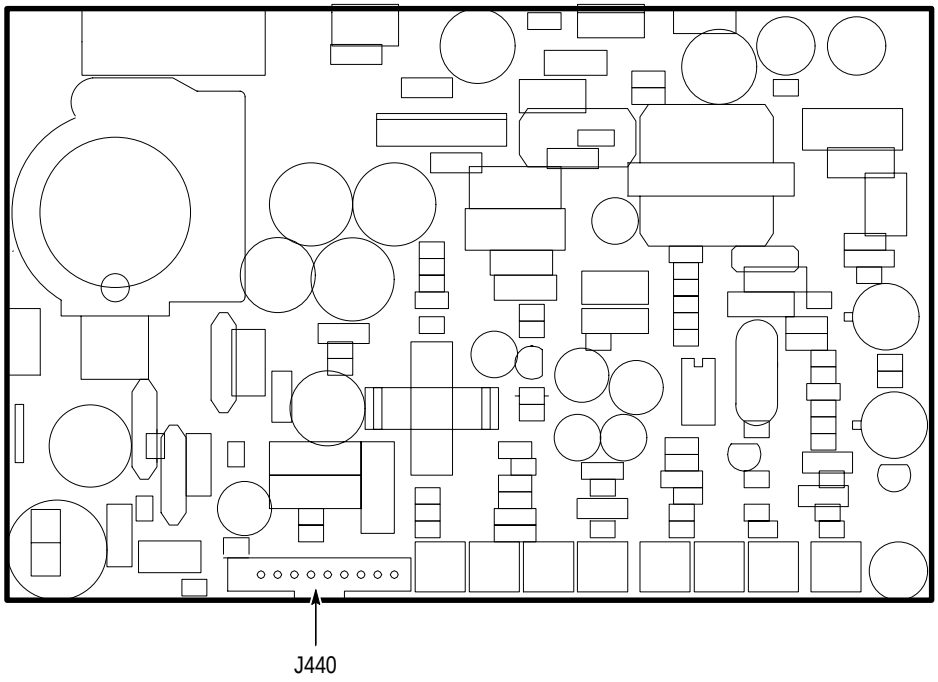


Figure 6–44: Monitor Connector J440

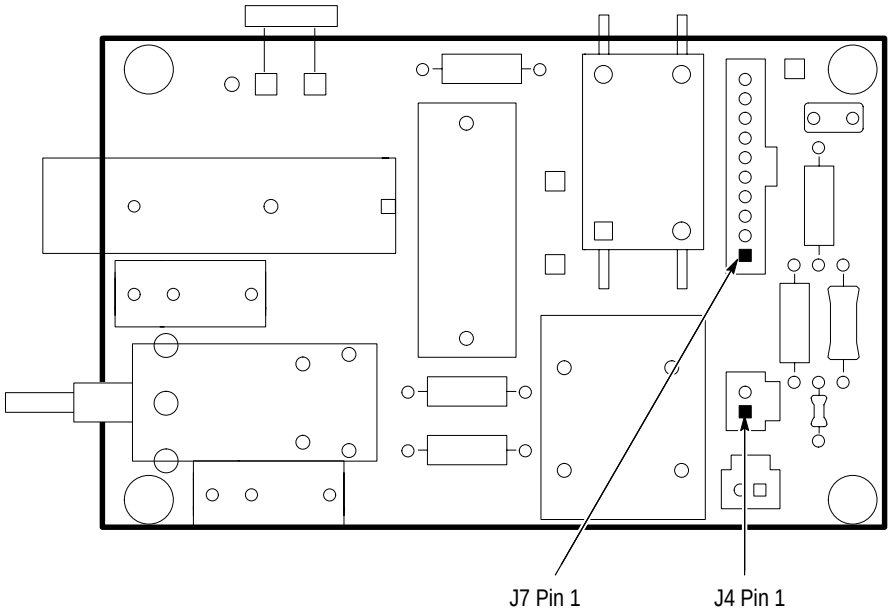


Figure 6–45: Auxiliary Power Connectors J4 and J7

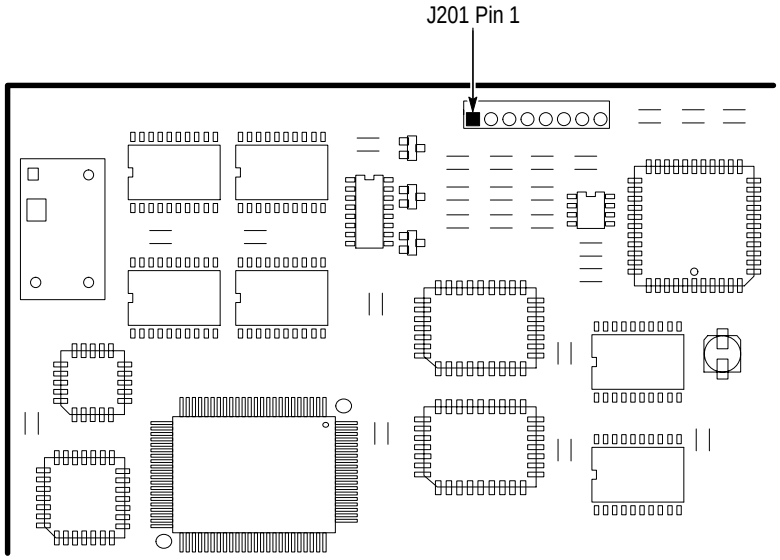


Figure 6–46: Display Connector J201

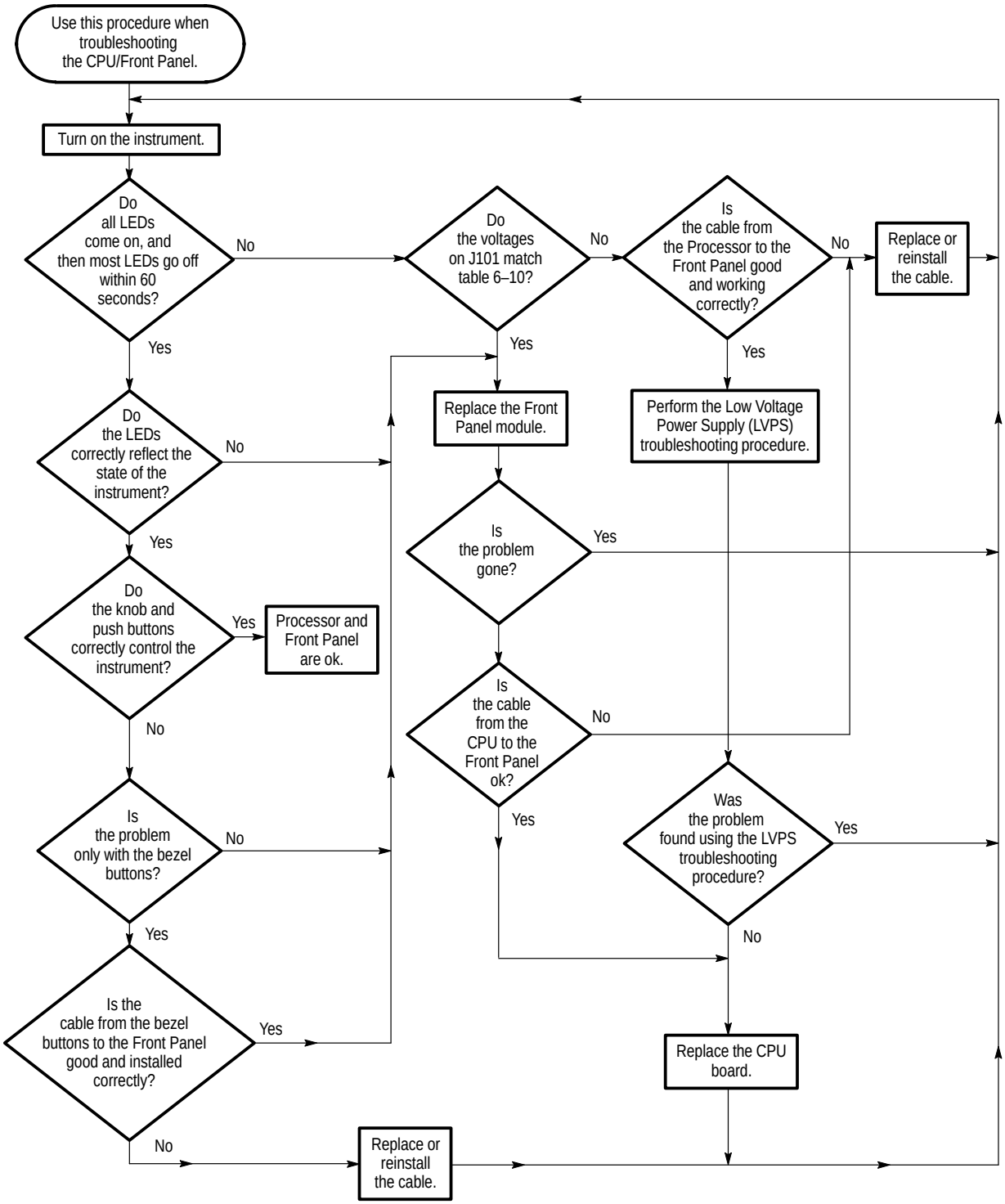


Figure 6–47: CPU/Front Panel Troubleshooting Procedure

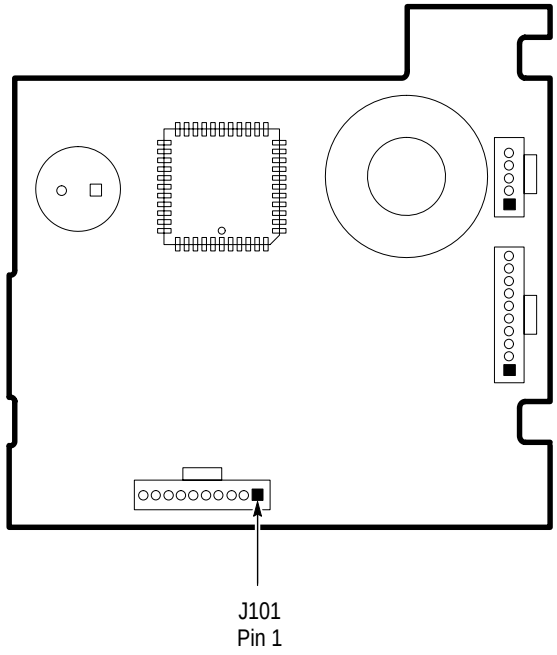


Figure 6–48: Front Panel Board Power Connector J101

Table 6–10: Front Panel Connector Voltages

Connector	Pin	Nominal Voltage
J101	Pins 2 and 4	5.1 V

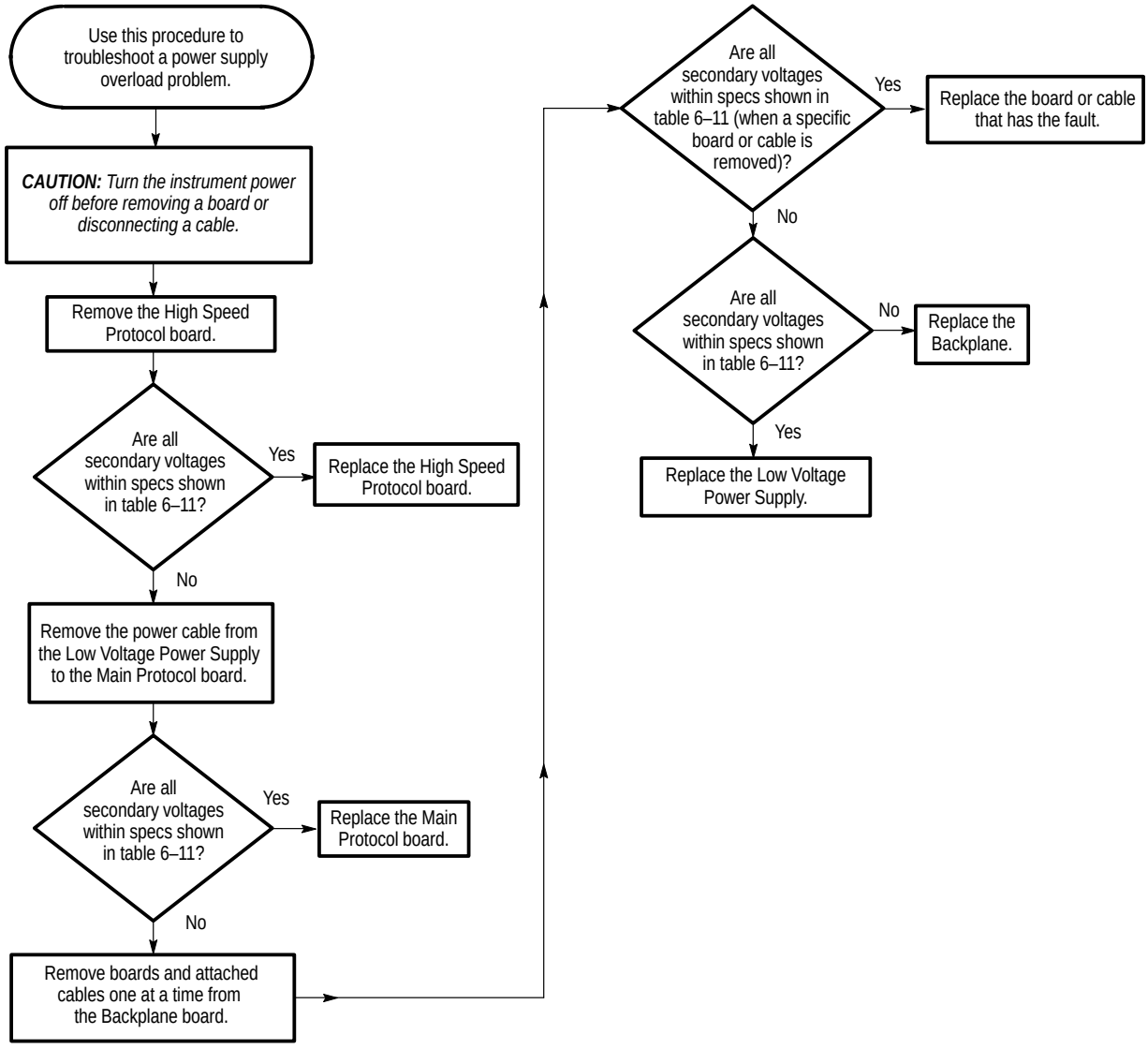


Figure 6–49: Low Voltage Power Supply Overload Troubleshooting Procedure

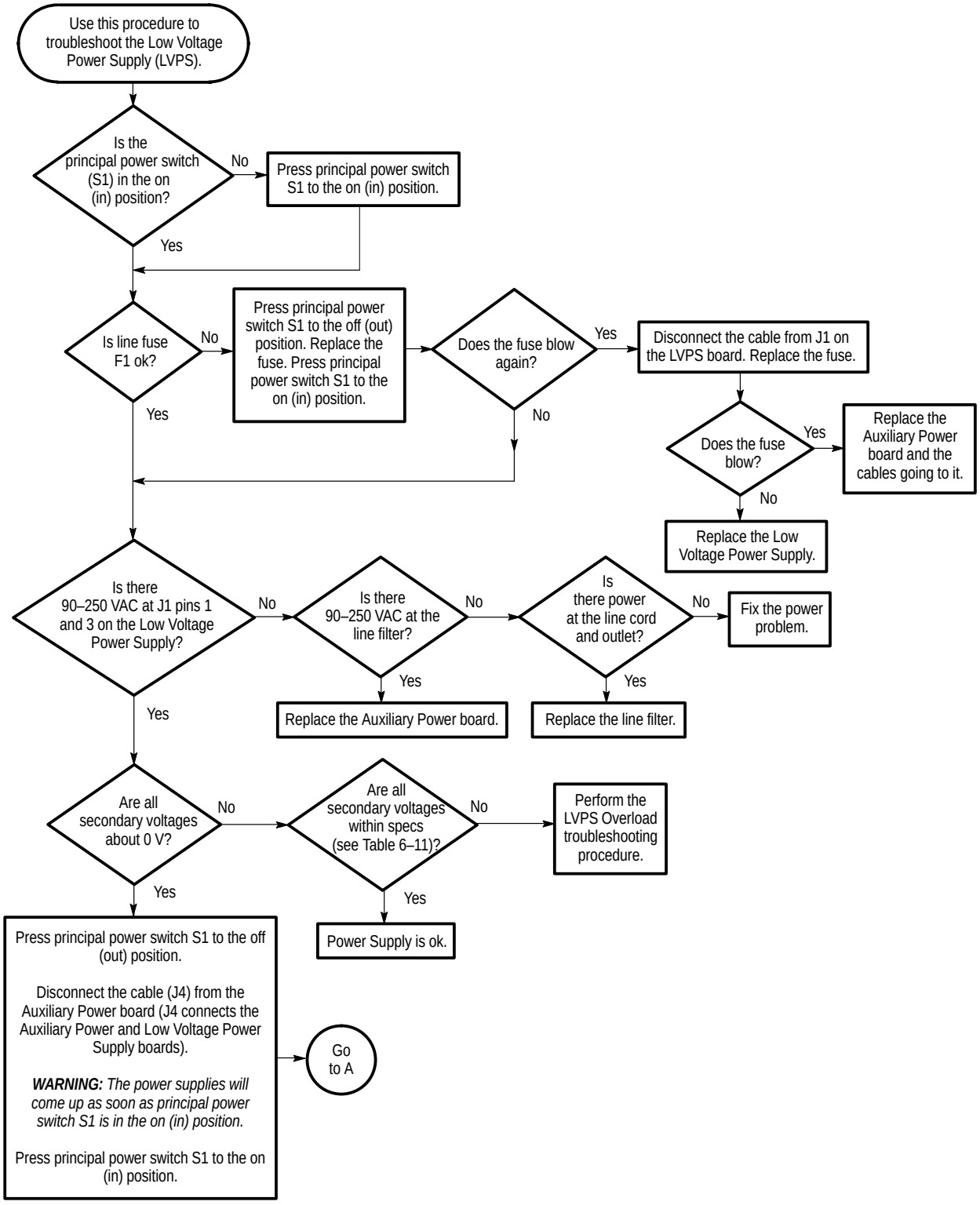


Figure 6–50: Low Voltage Power Supply Troubleshooting Procedure

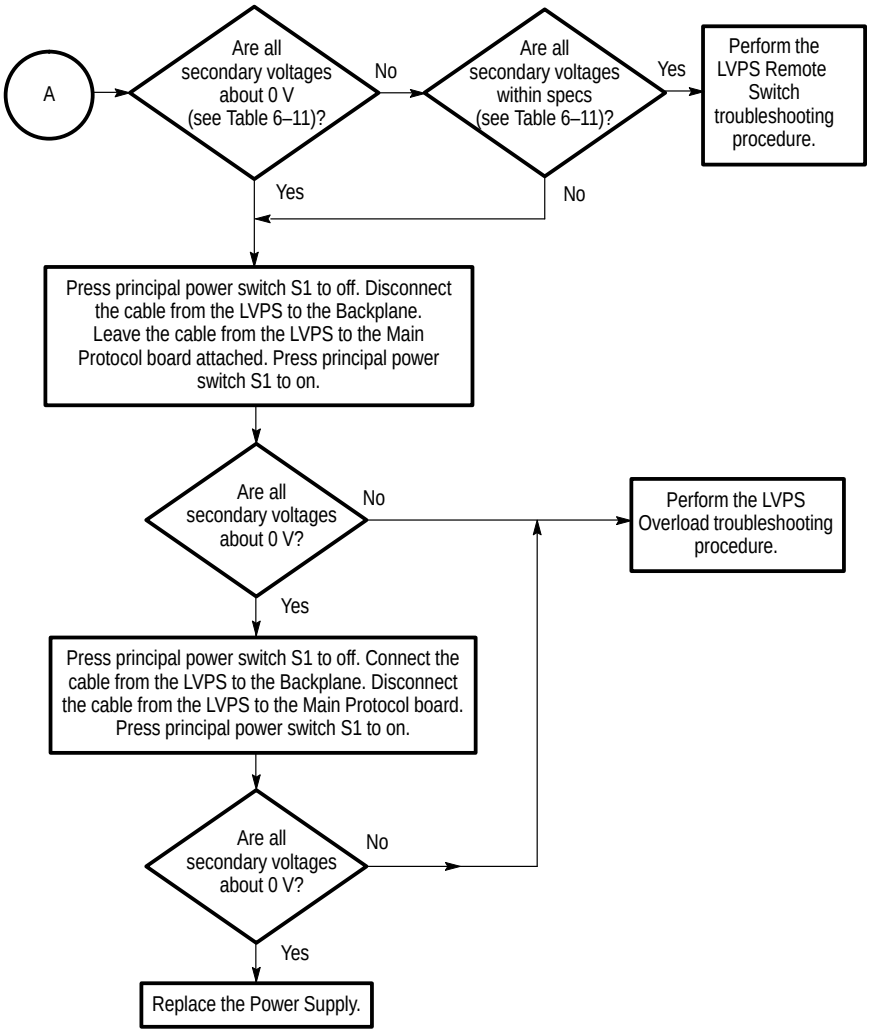


Figure 6–50: Low Voltage Power Supply Troubleshooting Procedure (Cont.)

Table 6–11: Normal Secondary Voltages

Supply	J15 Pin	Minimum Output	Maximum Output
+5.1 V	7	+5.05 V	+5.15 V
+15 V	3	+14.85 V	+15.15 V
–6.4 V	5	–6.35 V	–6.45 V
–15 V	1	–14.85 V	–15.15 V

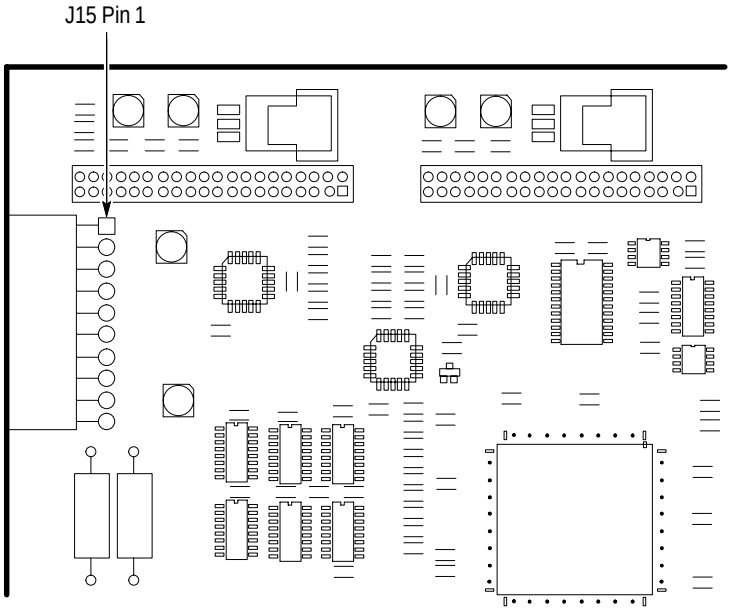


Figure 6–51: Main Protocol Board

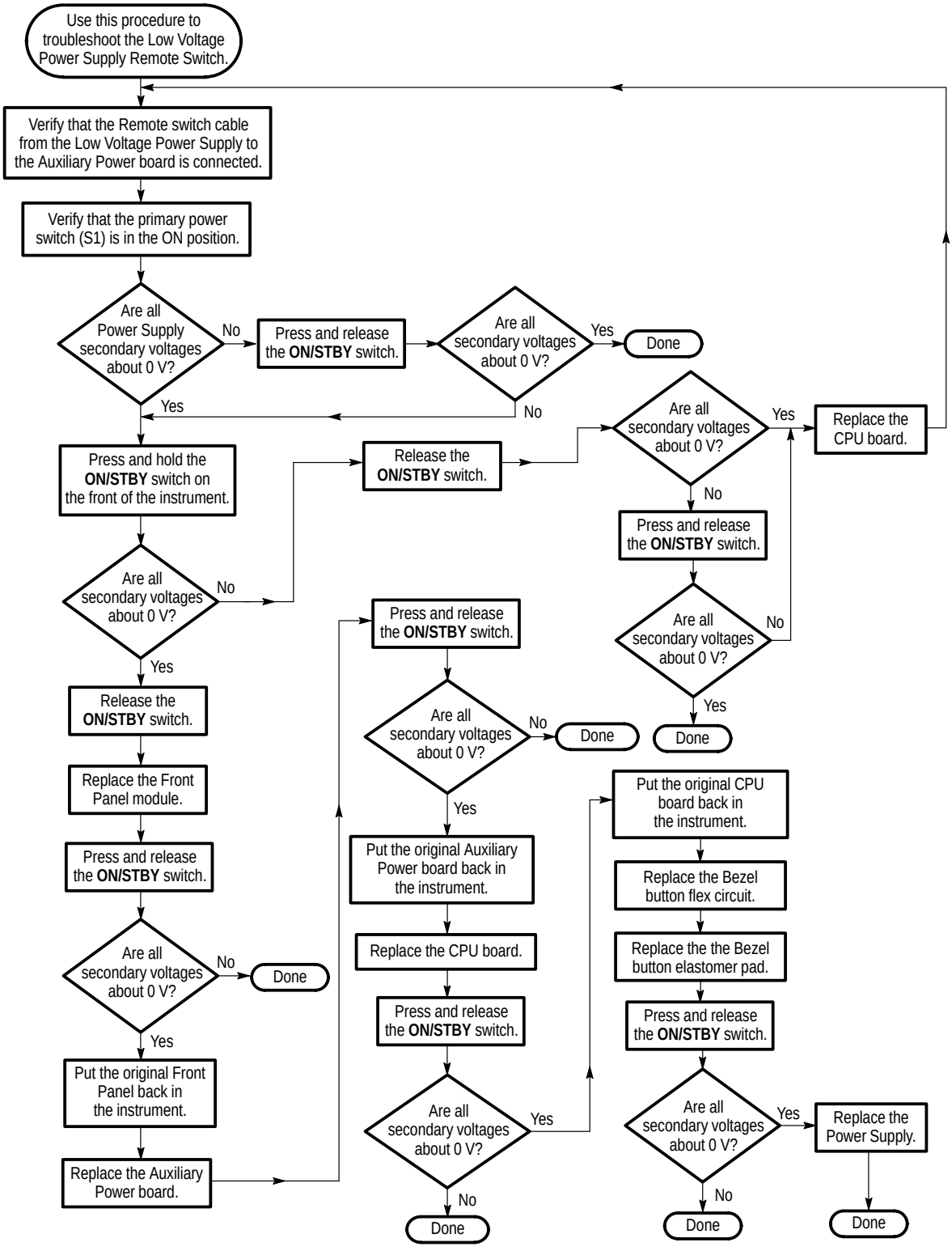


Figure 6–52: Low Voltage Power Supply Remote Switch Troubleshooting Procedure

Shared Routines

There are several routines that are shared by the diagnostic tests. Although you cannot invoke these shared routines individually, you might encounter error messages that originate with the shared routines. The following entries describe the shared routines.

RAM Data Line Routine

This general routine is used by various tests. The routine performs a walking-1's exercise on the specified memory location.

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Addr: 0xXXXXXX, Exp: 0xXX, Act: 0xXX
```

The "Addr" field contains the address where the fault was detected. The "Exp" field contains the expected value and the "Act" field contains the actual data read from memory.

RAM Address/Data Routine

This general routine is used by various tests. The routine performs an address line/data pattern verification on the specified band of memory.

Error Messages.

Test FAIL:

```
Addr: 0xXXXXXX, Exp: 0xXX, Act: 0xXX
```

The "Addr" field contains the address where the fault was detected. The "Exp" field contains the expected value and the "Act" field contains the actual data read from memory.

Bus Errors Routine

This section describes the error messages produced due to a bus error during diagnostics.

When diagnostics are invoked, the diagnostics system swaps in its own bus error interrupt handler to trap any bus faults that may occur while testing. The diagnostic version of the bus error handler performs the following steps upon detecting a bus fault:

- Records the address of the location where the bus fault occurred.
- Performs back-to-back reads of the Protocol Board STTX Identity Register.
- Determines if any delay should be performed and prints a message to the VxWorks console port if performing a delay.

The individual test routines do not necessarily know whether or not a bus error occurred. The tests simply run to completion. The diagnostic control program checks if a bus error occurred at the completion of each test. Then, if a bus error did occur the Error Message described below is produced. The occurrence of a bus fault takes higher precedence than a test failure (since the bus error may be the source of the failure). Therefore if a test fails and a bus error occurred during the test, the diagnostics system will only report the error message describing the bus error.

The STTX Identity register on the protocol board contains information on the presence (or absence) of the various clocks. If a bus error occurred due to protocol hardware, this information may be useful. Therefore the diagnostic error message reports the contents of this register.

Error Messages. Potential error messages are as follows:

```
BUS ERROR At Addr: 0xXXXXXX, (STTX Reg 3: 0xXX)
```

The “Addr” field contains the address where the bus fault occurred. The “STTX Reg 3” field contains the contents of the STTX Identity register.

verifyADC(channel, minVal, maxVal) Routine

This general routine is used to verify the output of a specified A/D channel falls within an allowed tolerance range. The exercise expects the following parameters:

- A/D Channel Number (0–7)
- Minimum Limit (mV)
- Maximum Limit (mV)

The exercise attempts to correct for errors in the A/D circuitry by also digitizing the ground and +2.5 V reference signals.

Error Messages. Potential error messages are as follows:

Test FAIL – A/D Completion:

The following error message is produced if the A/D converter fails to complete within the expected duration. The “Addr” and “Exp” fields define the register address and bit position of the A/D completion status bit.

```
Addr: 0x9B0000, Exp: 0x8000, Act: 0x0
```

Test FAIL – Limits:

The following error message is produced if the digitized signal does not fall within the allowed tolerance range. All values are reported in mV.

```
Min: X, Max: X, Act: X
```

loopbackHwInit() Routine

This routine places the protocol hardware in a quiescent state from which all loopback tests begin.

Error Messages. None.

loopbackTest(rate, type) Routine

This routine provides the main exercise of the protocol hardware. The routine programs the transmitter and receiver identically, then verifies the hardware is running error-free (no failures/alarms/errors). The routine assumes the loopback connection was made (either externally or internally) prior to invoking this routine. Once the integrity of the loopback path is checked, the test then verifies the hardware's ability to generate and detect various error conditions (single BIP errors and pointer movements).

The routine expects the following parameters:

- Line Rate (STS-1, STS-3, STS-12)
- Type (Electrical, Optical)

The routine exercises all possible structure/channel combinations for the specified rate.

Notes. Not indicated in the above description is how the test runs when invoked as part of the Self Test suite. To speed things up during self test, the exercise is not as exhaustive. The rate/structure/channel combinations exercised as part of self test are:

- 52Mb, STS-1 Structure, Channel 1
- 155Mb, STS-3c Structure, Channel 1
- 622Mb, STS-3c Structure, Channels 1–4

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the hardware reports an unexpected failure, alarm, or error condition. The "Exp" field will be 0 if the test was checking for an error-free state. During the error insertion portion of the routine the field indicates the number of expected errors. The "Act" field indicates the

number of errors reported by the hardware. For failures/alarms this value is 1. For errors, however, the value is a count read from the hardware.

```
<RATE_ID> <HW_STATUS>, Exp: 0xX, Act: 0xX

      Where <RATE_ID>:
            "Elec 52Mb", "Elec 155Mb", "Elec 622 Mb",
            "Opt 52Mb", "Opt 155Mb", "Opt 622 Mb",
            "Elec 52Mb (c)", "Elec 155Mb (c)",
            "Elec 622Mb (c)",
            "Opt 52Mb (c)", "Opt 155Mb (c)",
            "Opt 622Mb (c)"

            [(c) indicates concatenated structure]

      Where <HW_STATUS>:
            "LOS", "LOF", "LOP",
            "(L/MS) AIS Alarm", "PAIS Alarm",
            "(L/MS) FERF Alarm", "PFERF Alarm",
            "Pattern Loss",
            "B1 Error", "B2 Error", "B3 Error",
            "Path FEBE Error", "Payload Error",
            "SPE/AU Pos Ptr Adj", "SPE/AU Neg Ptr Adj"

Ex:
      Opt 52Mb LOP, Exp: 0x0, Act: 0x1

      The instrument was running at optical 52Mb
      rate, STS-1 structure and detected a LOP
      condition.
```

Tributary Shared Routines

There are several routines that are shared by tributary diagnostic tests. Although you cannot invoke these shared routines individually, you might encounter error messages that originate with the shared routines. The following entries describe the shared routines.

tribInit() This routine is responsible for initializing the tributary board; including loading either the DSn/En XILINX.

Error Messages. Potential error messages are as follows:

Test FAIL – tribInit():

The following error message is produced if the tributary hardware load XILINX failed for either the DSn or En rate.

```
Load XILINX failure, Exp: 0x0, Act: 0x1
```

protoInit()

This routine is responsible for initializing both the tributary board and the protocol board. The initialization of the tributary board is performed by calling tribInit().

The routine initializes both the tributary board and the protocol board. After the initialization is complete, the tributary board is then connected to the Com Bus.

Error Messages. Potential error messages are as follows:

Test FAIL – protoInit():

The following error message is produced if the protocol hardware failed to initialize properly. A LOS, LOF, or LOP is present at the protocol loopback. This can be due to an STTX failure.

```
Elec 52Mb LOS/LOF/LOP, Exp: 0x0, Act: 0x1
```

The following error message is produced if the ADMA failed to initialize without any DS1 BIT errors.

```
ADMA failed to initialize, Exp: 0x0, Act: 0x1
```

diagGroupTestSet (Tributary Rate)

This routine provides the main exercise for the tributary hardware test set. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

To test the ability of the test set to generate and receive various DSn/En alarms (AIS, YELLOW, REMOTE), the routine loops through all the available DSn/En alarms and verify that each of these can be transmitted and received.

To verify that the test set can generate and receive various DSn/En errors (BIT, FRAME, CRC, C-Bit, P-Bit), the routine loops through all the available DSn/En errors and verifies that each of these can be transmitted and received.

To test the various DSn/En framing formats (UNFRAMED, SF, ESF, C-BIT, M13, PCM30, PCM31, PCM30CRC, PCM31CRC, FRAMED), the routine programs the transmitter and receiver identically, then verifies that the hardware is running error-free (no failures/alarms/errors). Once the integrity of the loopback path is checked, the test then verifies the ability of the test set to generate and detect pattern bit errors.

To verify the ability of the test set to generate and receive a DSn/En pattern (PRBS23), the routine first programs the transmitter and receiver to the same pattern. It then verifies that pattern lock is present. Finally, the receiver is then programmed to a different pattern, and it then verifies that pattern lock is not present. The routine expects the following parameters: diagGroupTestSet (DS1, DS3, E1, E3).

The routine exercises the ability of the tributary hardware to generate and receive DSn/En alarms, errors, framing formats, and patterns.

Error Messages. Potential error messages are as follows:

Test FAIL – Initialization:

Refer to *tribInit*, on page 6–89, for a list of possible error messages during initialization.

Test FAIL – diagTribTestSetAlarms():

The following error message is produced if the hardware expected to see a specific DSn/En alarm, but the alarm was not present.

```
<ALARM>, Exp: 0x1, Act: 0x0

      Where <ALARM>:
            "AIS", "Yellow", "Remote",
```

The following error message is produced if the hardware expected to see no alarms, but instead a DSn/En alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

      Where <ALARM>:
            "AIS", "Yellow", "Remote"
```

Test FAIL – diagTribTestSetErrors():

The following error message is produced if the number of DSn/En errors inserted does not equal the number of DSn/En errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
<ERROR>, Exp: 0xX, Act: 0xX

      Where <ERROR>:
            "Bit", "Frame", "CRC", "CBIT CP", "P-Bit",
```

Test FAIL – diagTribTestSetFraming():

The following error message is produced if the hardware expected to see no alarms, but instead a DSn/En alarm is present.

```
<FRAMING FORMAT>, <ALARM>, Exp: 0x0, Act: 0x01

      Where <FRAMING FORMAT>:
            "Unframed", "Super Frame",
            "Ext. Super Frame", "C Bit", "M13",
            "PCM30", "PCM31", "PCM30 CRC",
            "PCM31 CRC", "Framed"

      Where <ALARM>:
            "AIS", "Yellow", "Remote"
```

The following error message is produced if the the hardware expected to see no DSn/En errors, but instead a DSn/En error is present. The “Act” field indicates the number of errors reported by the hardware.

```
<FRAMING FORMAT>, <ERROR>, Exp: 0x0, Act: 0xX

      Where <FRAMING FORMAT>:
            "Unframed", "Super Frame",
            "Ext. Super Frame", "C Bit", "M13",
            "PCM30", "PCM31", "PCM30 CRC",
            "PCM31 CRC", "Framed"

      Where <ERROR>:
            "Bit", "Frame", "CRC", "CBIT CP", "P-Bit"
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of DSn/En BIT errors reported by the hardware. The “Exp” field indicates the number of DSn/En BIT errors expected.

```
<FRAMING FORMAT>, <Bit>, Exp: 0x0, Act: 0xX

      Where <FRAMING FORMAT>:
            "Unframed", "Super Frame",
            "Ext. Super Frame", "C Bit", "M13",
            "PCM30", "PCM31", "PCM30 CRC",
            "PCM31 CRC", "Framed"
```

Test FAIL – diagTribTestSetPatterns():

The following error message is produced if the hardware expected to see a pattern lock, but no pattern lock was present.

```
TX/RX Pat: PRBS23, Pat. Lock, Exp: 0x1, Act: 0x0
```

The following error message is produced if the hardware expected to see no pattern lock, but a pattern lock was present.

```
Tx/Rx Pat: Diff., Pat. Lock, Exp: 0x0, Act: 0x1
```

diagGroupLineInterface (Tributary Rate, Loopback)

This routine tests the connection between the test set and the line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

To test the ability of the line interface to detect an LOS condition, the routine first programs the transmitter and receiver identically. It then verifies that a valid DSn/En signal is received. Finally, the connection between the test set and line interface is broken, and it then verifies that an LOS condition is present.

To test the various line codings, the routine programs the transmitter and receiver identically, then verifies the hardware is running error free (no failures/alarms/errors). Once the integrity of the loopback path is checked, the test then verifies the ability of the hardware to generate and detect pattern bit errors. The routine diagGroupLineInterface expects the following parameters: Tributary Rate (DS1, DS3, E1, E3, E4)loopback (Internal, External).

The routine tests the ability of the line interface to detect an LOS, and its ability to generate and receive all possible line coding formats.

Error Messages. Potential error messages are as follows:

Test FAIL – Initialization:

Refer to *tribInit*, on page 6–89, for a list of possible error messages during initialization.

Test FAIL – diagLineInterfaceLos():

The following error message is produced if the hardware expected to see a DSn/En signal, but a LOS was detected.

```
LOS, Exp: 0x0, Act: 0x1
```

The following error message is produced if the hardware expected to see a LOS status, but a valid DSn/En signal was detected.

```
LOS, Exp: 0x1, Act: 0x0
```

Test FAIL – diagLineInterfaceCode():

The following error message is produced if the hardware expected to see no alarms, but a DSn/En alarm is present.

```
<LINE_CODING>, <ALARM>, Exp: 0x0, Act: 0x1

       Where <LINE_CODING>:
              "AMI", "B8ZS", "HDB3", "B3ZS", "CMI"

       Where <ALARM>:
              "AIS", "Yellow", "Remote"
```

The following error message is produced if the hardware expected to see no errors, but a DSn/En error is present. The “Act” field indicates the number of errors reported by the hardware.

```
<LINE_CODING>, <ERROR>, Exp: 0x0, Act: 0xX

       Where <LINE_CODING>:
              "AMI", "B8ZS", "HDB3", "B3ZS", "CMI"

       Where <ERROR>:
              "Bit", "Frame", "CRC", "CBIT CP", "P-BIT",
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of bit errors reported by the hardware. The “Exp” field indicates the number of bit errors expected.

```
<LINE_CODING>, >ERROR>, Exp: 0xX, Act: 0xX

       Where <LINE_CODING>:
              "AMI", "B8ZS", "HDB3", "B3ZS", "CMI"

       Where <ERROR>:
              "Bit", "Frame", "CRC", "CBIT CP", "P-BIT"
```

diagGroupMapDemap (Tributary Rate)

This routine tests the connection between the test set and the mapper/demapper. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

To test the ability of the mapper/demapper to generate and receive various VT/TU alarms and failures (VT AIS, VT YELLOW, VT LOP, VT LOM), the routine loops through all the available VT/TU alarms and failures and verifies that each of these can be transmitted and received.

To verify that the mapper/demapper can generate and receive various VT/TU errors (VT BIP, VT FEBE), the routine loops through all the available VT/TU errors and verifies that they can be transmitted and received.

To test the ability of the mapper/demapper to switch between active VT/TU channels, the routine programs the transmitter and receiver to the same active VT/TU channels. Then the test verifies that the mapper/demapper can transmit and detect VT/TU BIP errors.

To verify that the mapper/demapper can generate background VT/TU patterns, the routine programs the active VT/TU channel to contain a PRBS23 pattern and the inactive VT/TU channel to a different pattern (QRSS or PRBS15). The receiver is then set to the active VT/TU channel and a pattern lock is verified with a PRBS23 pattern. Finally, the receiver is set to the inactive VT/TU channel and a pattern lock is verified for either a QRSS or PRBS15 pattern (depending on the DSn/En rate).

To verify that the mapper/demapper can generate background VT/TU framing formats, the routine programs the active and inactive VT/TU channel to a set framing format. Then the routine switches the receiver between the active and inactive VT/TU channels and verifies that the expected framing format is present. For VT channels, the active channel framing format is set to unframed and the inactive VT channel framing format is set to extended super frame. For TU channels, the active and inactive channel framing formats are set to PCM30CRC (TU–12) or framed (TU–3).

Finally, the routine also verifies that the mapper/demapper can map and demap DSn/En alarms and errors. To do this, the transmitter and receiver are programmed identically. The integrity of the loopback is verified by checking for a pattern lock. Then the test generates DSn/En errors and alarms. The routine expects the following parameters: (DS1, DS3, E1, E3, E4).

The routine exercises the ability of the tributary hardware to map/demap DSn/En signals. The test generates and receives VT/TU alarms, failures, errors, framing formats, and patterns.

Error Messages. Potential error messages are as follows:

Test FAIL – Initialization():

Refer to protoInit, on page 6–90, for a list of possible error messages during initialization.

Test FAIL – diagTribMapDemapFailures():

The following error message is produced if the hardware expected no VT/TU failures, but a VT/TU failure is present.

```
<FAILURE>, Exp: 0x0, Act: 0x1

      Where <FAILURE>:
            "VT LOP", "VT LOM"
```

The following error message is produced if the hardware expected a specific VT/TU failure, but the failure was not present.

```
<FAILURE>, Exp: 0x1, Act: 0x0

       Where <FAILURE>:
              "VT LOP", "VT LOM"
```

Test FAIL – diagTribMapDemapAlarms():

The following error message is produced if the hardware expected no VT/TU alarms, but instead a VT/TU alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

       Where <ALARM>:
              "VT AIS", "VT Yellow"
```

The following error message is produced if the hardware expected a specific VT/TU alarm, but the alarm was not present.

```
<ALARM>, Exp: 0x1, Act: 0x0

       Where <ALARM>:
              "VT AIS", "VT Yellow"
```

Test FAIL – diagTribMapDemapErrors():

The following error message is produced if the number of VT/TU errors inserted does not equal the number of VT/TU errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
<ERROR>, Exp: 0xX, Act: 0xX

       Where <ERROR>:
              "VT BIP", "VT FEBE"
```

Test FAIL – diagTribMapDemapChannels():

The following error message is produced if the number VT/TU BIP errors inserted does not equal the number of VT/TU BIP errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
VT BIP, Exp: 0xX, Act: 0xX
```

Test FAIL – diagTribMapDemapBckgndData():

The following error message is produced if the hardware expected a pattern lock on either the active channel or background channel, but no pattern lock was present.

```
<CHANNEL>, Pattern Lock, Exp: 0x1, Act: 0x0
       Where <CHANNEL>:
              "Act Ch.", "Bckgnd Ch."
```

Test FAIL – diagTribMapDemapBckgndFraming():

The following error message is produced if the hardware expected no VT/TU errors, but a VT/TU error is present. The “Act” field indicates the number of errors reported by the hardware.

```
<FRAMING FORMAT>, <ERROR>, Exp: 0x0, Act: 0xX
       Where <FRAMING FORMAT>
              "Unframed", "Ext. Super Frame",
              "PCM30 CRC", "Framed"

       Where <ERROR>
              "VT BIP", "VT FEBE"
```

Test FAIL – diagTribMapDemapTestSet():

The following error message is produced if the hardware expected a pattern lock, but no pattern lock was present.

```
Pattern Lock, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of DSn/En errors inserted does not equal the number of DSn/En errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
<ERROR>, Exp: 0xX, Act: 0xX
       Where <ERROR>
              "Bit", "Frame"
```

The following error message is produced if the hardware expected an E4 AIS alarm, but the alarm was not present.

```
AIS, Exp: 0x1, Act: 0x0
```

diagTribRing (Tributary Rate)

This routine verifies the overall operation of the tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various VT/TU and DSn/En alarms, errors, and failures are tested. The routine expects the following parameters: diagTribRing (DS1, DS3, E1, E3, E4).

The routine tests the ability of the tributary hardware to generate and receive VT/TU and DSn/En alarms, errors, and failures.

Error Messages. Potential error messages are as follows:

Test FAIL – diagTribRing():

The following error message is produced if the hardware expected a pattern lock, but instead no pattern lock was present.

```
Pattern Lock, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of BIT errors reported by the hardware. The “Exp” field indicates the number of BIT errors expected.

```
Bit, Exp: 0xX, Act: 0xX
```

The following error message is produced if the hardware expected a DSn/En AIS alarm, but the alarm was not present.

```
AIS, Exp: 0x1, Act: 0x0
```

The following error message is produced if the hardware expected no DSn/En alarms, but a DSn/En alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

      Where <ALARM>:
            "AIS", "Yellow", "Remote"
```

The following error message is produced if the hardware expected no VT/TU alarms, but a VT/TU alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

      Where <ALARM>:
            "VT AIS", "VT Yellow"
```

The following error message is produced if the hardware expected no VT/TU failures, but a VT/TU failure is present.

```
<FAILURE>, Exp: 0x0, Act: 0x1

      Where <FAILURE>:
            "VT LOP", "VT LOM"
```

The following error message is produced if the hardware expected a VT/TU Yellow alarm, but the alarm was not present.

```
VT Yellow, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of VT/TU BIP errors inserted does not equal the number of VT/TU BIP errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
VT BIP, Exp: 0xX, Act: 0xX
```

Diagnostic Test Descriptions

The following diagnostic test descriptions include the name of the test, a short description, a command line which can be used to invoke the test via GPIB, and a list of error messages that the test can generate. Table 6–12 summarizes the diagnostic tests available.

Table 6–12: Diagnostic Test Summary

Test Group	Tests		
Self Test (Power-Up)	Refer to Table 6–13, on page 6–101, for a list of tests.		
System Internal	Refer to Table 6–14, on page 6–102, for a list of tests.		
System External	Refer to Table 6–15, on page 6–105, for a list of tests.		
Protocol	Misc Register SETI Register Register Access Flash Voltage Flash Checksum	ITX RAM IRX RAM PRX RAM IRX FIFO A/D Converter	Power Supply 52Mb Loop 155Mb Loop 622Mb Loop
Clock	Internal Reference Freq Offset		
O/E Module	Status Identification Access Tx Optical Power	Rx Signal Level Internal 52Mb Loop Internal 155Mb Loop Internal 622Mb Loop	External 52Mb Loop External 155Mb Loop External 622Mb Loop

Table 6–12: Diagnostic Test Summary (Cont.)

Test Group	Tests		
Tributary	Trib Register Access Trib Flash Voltage Trib Flash Checksum Trib DS1 Test Set Trib DS3 Test Set Trib DS1 Line Interface (Internal) Trib DS3 Line Interface (Internal) Trib DS1 Line Interface (External) Trib DS3 Line Interface (External)	Trib DS1 Map/Demap Trib DS3 Map/Demap Trib DS1 Ring Trib DS3 Ring Trib E1 Test Set Trib E3 Test Set Trib E1 Line Interface (Internal) Trib E3 Line Interface (Internal) Trib E4 Line Interface (Internal)	Trib E1 Line Interface (External) Trib E3 Line Interface (External) Trib E4 Line Interface (External) Trib E1 Map and Demap Trib E3 Map and Demap Trib E4 Map and Demap Trib E1 Map Ring Trib E3 Map Ring
JAWA	Clock Recovery Circuit Register Access Flash Checksum DAC Loopback	Clock Recovery Divider Tracking PLL Meas Phase Detector Meas PLL Locking	Meas PLL Gain FIFO Analog Output
JAWG	Wander Loop Locking Jitter Loop Locking	Jitter Loop Low-Pass Filters	Jitter Generation
CPU	Vector Interrupt IIC Control Clock/Calendar	Clk/Cal Battery DUART	
Display	Video RAM RAMDAC White Field	Grey Field White Box Test Grid	Composite HW Scrolling
Front Panel	Internal (Front Panel Self Test) LEDs	Speaker Manual (Interactive)	
Disk	PM110 Register PM110 Cache PM110 Counter	Controller Drive Format & Verify	Dysan Seek

Self Test

The Self Test group refers to the suite of tests that are invoked as part of the power-up process. These test routines are designed to verify the maximum amount of hardware in the minimum amount of time. The group provides thorough coverage of the hardware, but offers very little in the way of fault isolation.

The Self Test group is useful for catching intermittent power-up failures. If the instrument occasionally fails power-up diagnostics, it may be useful to loop on the Self Test diagnostics to verify the failure occurs. If a failure is then detected, it is recommended that the appropriate board-level suite of tests be invoked to aid in the fault isolation process. The first word of each failure message identifies the test group with which the routine is associated (e.g. Proto, O/E, etc.).

GPIB Command. *TST?

Table 6–13 lists the tests along with their corresponding test numbers that are invoked as part of the Self Test suite.

Table 6–13: Self Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Clk/Cal Battery	4	Processor Board
CPU DUART	5	Processor Board
Disk PM110 Reg	14	Disk Drive
Disk PM110 Cache RAM	15	Disk Drive
Disk PM110 Counter	16	Disk Drive
Disk Controller	17	Disk Drive
Disk Drive	18	Disk Drive
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto Power Supply	35	Protocol Board
Clk Internal Ref	39	Clock Board
O/E Status	41	Plug-In Interface Module
O/E Identification	42	Plug-In Interface Module
O/E Access	43	Plug-In Interface Module
O/E Tx Optical Power	44	Plug-In Interface Module

Table 6–13: Self Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
O/E Int 52Mb Loop	46	Plug-In Interface Module
O/E Int 155Mb Loop	47	Plug-In Interface Module
O/E Int 622Mb Loop	48	Plug-In Interface Module
Trib Flash Voltage	52	Tributary
Trib Flash Checksum	53	Tributary
Trib Map/Demap E4	73	Tributary
Trib Ring DS1	74	Tributary
Trib Ring DS3	75	Tributary
Trib Ring E1	76	Tributary
Trib Ring E3	77	Tributary
JAWA Flash Checksum	79	JAWA/JAWG

Error Messages. See the individual test descriptions for the explanation of possible failures.

System Internal Test

The System Internal group is similar to the Self Test group in that it is a collection of various tests, not just those specific to a single board. This group includes all tests that do not require user interaction or external cabling.

The purpose of the System Internal group is to provide a convenient way of running all internal diagnostics with a single command. This suite of tests is more thorough than the self test group and provides an exhaustive exercise of the instrument. By running this test group and verifying no faults were detected, the user should have a high level of confidence in the integrity of the instrument.

Table 6–14 lists the tests along with their corresponding test numbers that are invoked as part of the System Internal group.

Table 6–14: System Internal Diagnostic Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Clk/Cal Battery	4	Processor Board
CPU DUART	5	Processor Board
Display Video RAM	6	Display Board

Table 6–14: System Internal Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
Display RAMDAC	7	Display Board
Disk PM110 Reg	14	Disk Drive
Disk PM110 Cache RAM	15	Disk Drive
Disk PM110 Counter	16	Disk Drive
Disk Controller	17	Disk Drive
Disk Drive	18	Disk Drive
Proto Misc Reg	25	Protocol Board
Proto SETI Reg	26	Protocol Board
Proto Reg Access	27	Protocol Board
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto ITX RAM	30	Protocol Board
Proto IRX RAM	31	Protocol Board
Proto PRX RAM	32	Protocol Board
Proto IRX FIFO	33	Protocol Board
Proto A/D Conv.	34	Protocol Board
Proto Pwr Supply	35	Protocol Board
Proto Bd 52Mb Loop	36	Protocol Board
Proto Bd 155Mb Loop	37	Protocol Board
Proto Bd 622Mb Loop	38	Protocol Board
Clk Internal Ref	39	Clock Board
Clk Freq Offset	40	Clock Board
O/E Status	41	Plug-In Interface Module
O/E Identification	42	Plug-In Interface Module
O/E Access	43	Plug-In Interface Module
O/E Tx Optical Power	44	Plug-In Interface Module
O/E Int STS-1 Loop	46	Plug-In Interface Module
O/E Int STS-3 Loop	47	Plug-In Interface Module
O/E Int STS-12 Loop	48	Plug-In Interface Module
Trib Flash Voltage	52	Tributary
Trib Flash Checksum	53	Tributary
Trib Register Access	54	Tributary
Trib TestSet DS1	55	Tributary

Table 6–14: System Internal Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
Trib TestSet DS3	56	Tributary
Trib TestSet E1	57	Tributary
Trib TestSet E3	58	Tributary
Trib Line Int DS1	64	Tributary
Trib Line Int DS3	65	Tributary
Trib Line Int E1	66	Tributary
Trib Line Int E3	67	Tributary
Trib Line Int E4	68	Tributary
Trib Map/Demap DS1	69	Tributary
Trib Map/Demap DS3	70	Tributary
Trib Map/Demap E1	71	Tributary
Trib Map/Demap E3	72	Tributary
Trib Map/Demap E4	73	Tributary
Trib Ring DS1	74	Tributary
Trib Ring DS3	75	Tributary
Trib Ring E1	76	Tributary
Trib Ring E3	77	Tributary
JAWA/JAWG Register Access	78	JAWA/JAWG
JAWA Flash Checksum	79	JAWA/JAWG
JAWA FIFO	80	JAWA/JAWG
JAWA DAC Loopback	81	JAWA/JAWG
JAWA Clock Recovery Divider	82	JAWA/JAWG
JAWA Tracking PLL	83	JAWA/JAWG
JAWA Clock Recovery 2 Mb/s	84	JAWA/JAWG
JAWA Clock Recovery 8 Mb/s	85	JAWA/JAWG
JAWA Clock Recovery 34 Mb/s	86	JAWA/JAWG
JAWA Clock Recovery 140/155 Mb/s	87	JAWA/JAWG
JAWA Clock Recovery 52 Mb/s	88	JAWA/JAWG
JAWA Clock Recovery 622 Mb/s	89	JAWA/JAWG
JAWA Meas Phase Detector	90	JAWA/JAWG
JAWA Meas PLL Locking	91	JAWA/JAWG
JAWA Meas PLL Gain	92	JAWA/JAWG
JAWA Analog Output	93	JAWA/JAWG

Table 6–14: System Internal Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
JAWG Jitter Loop Low-Pass Filter	94	JAWA/JAWG
JAWG Wander Loop Locking	95	JAWA/JAWG
JAWG Jitter Loop Locking	96	JAWA/JAWG
JAWG Jitter Generation	97	JAWA/JAWG

GPIB Command. DIAG:SELECT SYSINTERNAL

Error Messages. See the individual test descriptions for the explanation of possible failures.

System External Test

The System External group is a super set of the System Internal group. This test suite includes all of the same routines, plus additional tests that make use of external loopback cables.

As with the System Internal group, the purpose of the System External group is to provide the user a high level of confidence in the integrity of the hardware. By making use of external cables, the hardware is verified up to and including the connectors themselves.

Table 6–15 lists the tests along with their corresponding test numbers that are invoked as part of the System External group.

Table 6–15: System External Diagnostic Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Clk/Cal Battery	4	Processor Board
CPU DUART	5	Processor Board
Display Video RAM	6	Display Board
Display RAMDAC	7	Display Board
Disk PM110 Reg	14	Disk Drive
Disk PM110 Cache RAM	15	Disk Drive
Disk PM110 Counter	16	Disk Drive
Disk Controller	17	Disk Drive

Table 6–15: System External Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
Disk Drive	18	Disk Drive
Proto Misc Reg	25	Protocol Board
Proto SETI Reg	26	Protocol Board
Proto Reg Access	27	Protocol Board
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto ITX RAM	30	Protocol Board
Proto IRX RAM	31	Protocol Board
Proto PRX RAM	32	Protocol Board
Proto IRX FIFO	33	Protocol Board
Proto A/D Conv.	34	Protocol Board
Proto Pwr Supply	35	Protocol Board
Proto Bd 52Mb Loop	36	Protocol Board
Proto Bd 155Mb Loop	37	Protocol Board
Proto Bd 622Mb Loop	38	Protocol Board
Clk Internal Ref	39	Clock Board
Clk Freq Offset	40	Clock Board
O/E Status	41	Plug-In Interface Module
O/E Identification	42	Plug-In Interface Module
O/E Access	43	Plug-In Interface Module
O/E Tx Optical Power	44	Plug-In Interface Module
O/E Rx Signal Level	45	Plug-In Interface Module
O/E Ext STS-1 Loop	49	Plug-In Interface Module
O/E Ext STS-3 Loop	50	Plug-In Interface Module
O/E Ext STS-12 Loop	51	Plug-In Interface Module
Trib Flash Voltage	52	Tributary
Trib Flash Checksum	53	Tributary
Trib Register Access	54	Tributary
Trib TestSet DS1	55	Tributary
Trib TestSet DS3	56	Tributary
Trib TestSet E1	57	Tributary
Trib TestSet E3	58	Tributary
Trib Line Ext DS1	59	Tributary

Table 6–15: System External Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
Trib Line Ext DS3	60	Tributary
Trib Line Ext E1	61	Tributary
Trib Line Ext E3	62	Tributary
Trib Line Ext E4	63	Tributary
Trib Line Int DS1	64	Tributary
Trib Line Int DS3	65	Tributary
Trib Line Int E1	66	Tributary
Trib Line Int E3	67	Tributary
Trib Line Int E4	68	Tributary
Trib Map/Demap DS1	69	Tributary
Trib Map/Demap DS3	70	Tributary
Trib Map/Demap E1	71	Tributary
Trib Map/Demap E3	72	Tributary
Trib Map/Demap E4	73	Tributary
Trib Ring DS1	74	Tributary
Trib Ring DS3	75	Tributary
Trib Ring E1	76	Tributary
Trib Ring E3	77	Tributary
JAWA/JAWG Register Access	78	JAWA/JAWG
JAWA Flash Checksum	79	JAWA/JAWG
JAWA FIFO	80	JAWA/JAWG
JAWA DAC Loopback	81	JAWA/JAWG
JAWA Clock Recovery Divider	82	JAWA/JAWG
JAWA Tracking PLL	83	JAWA/JAWG
JAWA Clock Recovery 2 Mb/s	84	JAWA/JAWG
JAWA Clock Recovery 8 Mb/s	85	JAWA/JAWG
JAWA Clock Recovery 34 Mb/s	86	JAWA/JAWG
JAWA Clock Recovery 140/155 Mb/s	87	JAWA/JAWG
JAWA Clock Recovery 52 Mb/s	88	JAWA/JAWG
JAWA Clock Recovery 622 Mb/s	89	JAWA/JAWG
JAWA Meas Phase Detector	90	JAWA/JAWG
JAWA Meas PLL Locking	91	JAWA/JAWG
JAWA Meas PLL Gain	92	JAWA/JAWG

Table 6–15: System External Diagnostic Test Summary (Cont.)

Test Name	Test Number	Board (FRU)
JAWA Analog Output	93	JAWA/JAWG
JAWG Jitter Loop Low-Pass Filter	94	JAWA/JAWG
JAWG Wander Loop Locking	95	JAWA/JAWG
JAWG Jitter Loop Locking	96	JAWA/JAWG
JAWG Jitter Generation	97	JAWA/JAWG

GPIB Command. DIAG:SELECT SYSEXTERNAL

Error Messages. See the individual test descriptions for the explanation of possible failures.

Protocol: Misc Register Test

This test verifies the processor's ability to access the Misc Register located on the Main Protocol board.

GPIB Command. DIAG:SELECT:ROUTINE PROTOMISCREG

Notes. This test is destructive to the state of the protocol hardware and therefore re-initializes the Protocol board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data pattern read back from the hardware differs from the pattern written.

```
Addr: 0x9B0100, Exp: 0xX, Act: 0xX
```

Protocol: SETI Register Test

This test verifies the processor's ability to access the SETI Register located on the High-Speed Protocol board.

GPIB Command. DIAG:SELECT:ROUTINE PROTOSETI

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data pattern read back from the hardware differs from the pattern written.

```
Addr: 0x9B0C02, Exp: 0xX, Act: 0xX
```

Protocol: Register Access Test

This test verifies the processor's ability to access all of the Protocol board registers. The test provides a quick verification that the board is alive and the various components can be programmed.

The test separates the registers into two categories:

- Read-Only Registers
- Read/Write Registers

The two types of registers are exercised differently. The read-only register exercise does not make any pass/fail decisions based on the contents of the register but simply verifies the register can be read without generating a bus error.

The read/write register exercise is modeled after the standard RAM address-line/data pattern exercise. Each register requires a mask value as not all bits are R/W and some bits affect other registers.

GPIB Command. DIAG:SELECT:ROUTINE PROTOREG

Notes. This test is destructive to the state of the protocol hardware and therefore re-initializes the Protocol board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the exercise fails. The "Addr" field contains the address of the register that failed.

```
Addr: 0xX, Exp: 0xX, Act: 0xX
```

Protocol: Flash Voltage Test

This test verifies the V_{pp} flash EEPROM programming voltage is disabled.

GPIB Command. DIAG:SELECT:ROUTINE PROTOVFL

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message indicates the flash EEPROM programming voltage is enabled.

```
Addr: 0x9B0000, Exp: 0x0, Act: 0x1
```

Protocol: Flash Checksum Test

This test verifies the integrity of the protocol board flash EEPROM device using a standard checksum routine.

The checksum routine used is a simple 16-bit summation. The routine reads a 16-bit value from memory and adds it to a running checksum.

GPIB Command. DIAG:SELECT:ROUTINE PROTOCKSUM

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the calculated checksum (“Act”) does not match the value stored in memory (“Exp”).

```
Addr: 0xA8000C, Exp: 0xX, Act: 0xX
```

Protocol: ITX RAM Test

This test verifies the processor interface to the ITX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on both banks of ITX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOITX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory-mapped addresses the routine updates an auto-incrementing set of address counters internal to the ITX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the ITX RAM is: 0x01FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page 6–86.

Protocol: IRX RAM Test

This test verifies the processor interface to the IRX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on the entire bank of IRX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOIRX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory-mapped addresses the routine updates an auto-incrementing set of address counters internal to the IRX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the IRX RAM is: 0x00FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page 6–86.

Protocol: PRX RAM Test

This test verifies the processor interface to the PRX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on the entire bank of PRX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOPRX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory-mapped addresses the routine updates an auto-incrementing set of address counters internal to the PRX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the PRX RAM is: 0x00FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page 6–86.

Protocol: IRX FIFO Test

This test verifies the processor interface to the IRX FIFO RAM as well as the cell integrity of the memory. The routine simply fills the FIFO with an incrementing pattern, then reads out the data and verifies the values are correct.

***NOTE**. The CPU is only allowed to write to the FIFO RAM when the incoming data rate is STS-3.*

GPIB Command. DIAG:SELECT:ROUTINE PROTOFIFO

Error Messages. Potential error messages are as follows:

Test FAIL – FIFO Active:

The following error message is produced if the FIFO ACT line is asserted after instructing the hardware to halt:

```
FIFO ACTive Stuck High, Exp: 0x0, Act: 0x1
```

Test FAIL – Memory:

The following error message is produced if the data read back from the FIFO does not match the expected value. The “Addr” field indicates which entry in the FIFO contained the failure.

```
Addr: 0xXXXX, Exp: 0xXX, Act: 0xXX
```

Protocol: A/D Converter Test

This test verifies the functionality of the protocol A/D converter. The test verifies that the ADC correctly digitizes the ground and +2.5 V reference signals.

GPIB Command. DIAG:SELECT:ROUTINE PROTOADC

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page 6–87.

Protocol: Power Supply Test

This test uses the Power Supply Fault Detect (PSFD) signal on the Protocol board to verify the Protocol board and interface module power supplies.

GPIB Command. DIAG:SELECT:ROUTINE PROTOPS

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page 6–87.

Protocol: 52Mb Loop Test

This test verifies the protocol hardware at the 52 MHz data rate. The test uses the serial Tx to Rx loopback path on the Protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP52

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Protocol: 155Mb Loop Test

This test verifies the protocol hardware at the 155 MHz data rate. The test uses the Tx to Rx loopback path between the SETI and SERI components on the protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware. The exercise is repeated for both electrical (with CMI encoding) and optical (without CMI) paths.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP155

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Protocol: 622Mb Loop Test

This test verifies the protocol hardware at the 622 MHz data rate. The test uses the Tx to Rx loopback path between the SETI and SERI components on the Protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP622

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Clock: Internal Reference Test

This test verifies the Clock Generator board's ability to lock on to the internal reference clock.

GPIB Command. DIAG:SELECT:ROUTINE CLKREF

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Phase Lock Failure, Exp: 0x39, Act: 0xXX
```

The above error message is produced if the status of the phase lock loops do not match the expected state (all locked).

Clock: Freq Offset Test

This test verifies the ability of the clock generator board to force frequency offsets into the payload and line clocks.

GPIB Command. DIAG:SELECT:ROUTINE CLKFREQ

Error Messages. Potential error messages are as follows:

Test FAIL – Payload Loss:

The following error message is produced if after railing the payload frequency offset the phase lock loops are not in their expected state. The expected value should indicate that only the internal reference and line offset are locked.

```
Payload PLL Loss Failure, Exp: 0x09, Act: 0xXX
```

Test FAIL – Payload Restore:

The following error message is produced if the phase lock loops do not respond properly when attempting to restore lock on the payload offset.

```
Payload PLL Restore Failure Exp: 0x39, Act: 0xXX
```

Test FAIL – Line Loss:

The following error message is produced if after railing the line frequency offset the phase lock loops are not in their expected state. The expected value should indicate that only the internal reference and both payload offsets are locked.

```
Line PLL Lose Failure, Exp: 0x31, Act: 0xXX
```

Test FAIL – Line Restore:

The following error message is produced if the phase lock loops do not respond properly when attempting to restore lock on the line clock.

```
Line PLL Restore Failure, Exp: 0x39, Act: 0xXX
```

Plug-In Interface Module: Status Test

This test verifies the presence of the Plug-In Interface Module. The Protocol board contains a status bit that indicates whether or not an Plug-In Interface Module is recognized.

GPIB Command. DIAG:SELECT:ROUTINE INTSTAT

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message indicates the Protocol board did not detect the presence of an Plug-In Interface Module.

```
Addr: 0x9B0000, Exp: 0x0, Act: 0x1
```

Plug-In Interface Module: Identification Test

This test verifies the processor's ability to properly read the Plug-In Interface Module's ID register.

GPIB Command. DIAG:SELECT:ROUTINE INTID

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug-In Interface Module is present by performing the O/E Status Test.

Refer to *Plug-In Interface Module Status Test*, on page 6–114, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if an unknown ID value is reported by the Plug-In Interface Module. The "Act" field contains the ID value read from the hardware.

```
Unknown O/E Module, Exp: 0x7, Act: 0xX
```

Plug-In Interface Module: Access Test

This test verifies the processor's ability to properly access the Plug-In Interface Module for both reading and writing. Communication with the Plug-In Interface Module is done via the I^2C bus. The test uses the Transceiver Control register to perform the access verification.

GPIB Command. DIAG:SELECT:ROUTINE INTACCESS

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug-In Interface Module is present by performing the O/E Status Test. Refer to *Plug-In Interface Module Status Test*, on page 6–114, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data read back from the Plug-In Interface Module is different from the pattern sent. The "Exp" field contains the value written and the "Act" field contains the value read.

```
Addr: 0x72, Exp: 0xX, Act: 0xX
```

Plug-In Interface Module: Tx Optical Power Test

This test verifies the Plug-In Interface Module's optical transmitter by checking the optical power is within a defined tolerance range.

The routine connects the internal Tx to Rx loopback path and verifies the analog signal using the Protocol board A/D converter.

GPIB Command. DIAG:SELECT:ROUTINE INTOPTPWR

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug-In Interface Module is present by performing the O/E Status Test. Refer to *Plug-In Interface Module Status Test*, on page 6–114, for more information.

This test will return PASS without performing the exercise if an electrical-only module is installed.

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page 6–87.

Plug-In Interface Module: Rx Signal Level Test

This test verifies the receive signal levels for both optical and electrical inputs. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

The test uses the A/D converter on the Protocol board to verify the electrical amplitude and optical power of the received signals.

GPIB Command. DIAG:SELECT:ROUTINE INTRXLEV

Notes. Requires user interaction.

Before proceeding with the remainder of the test, this routine first verifies that the Plug-In Interface Module is present by performing the O/E Status Test. Refer to *Plug-In Interface Module Status Test*, on page 6–114, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL – No Signal:

The following error message is produced if the Plug-In Interface Module does not detect an active input signal. (The ACTIVE SIGNAL status bit is active low.)

```
Active Signal Not Detected, Exp: 0x0, Act: 0x1
```

For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page 6–87.

Plug-In Interface Module: Internal 52Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 52 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP52I

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Plug-In Interface Module: Internal 155Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 155 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP155I

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Plug-In Interface Module: Internal 622Mb Loop Test

This test verifies the optical data path at the 622 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP622I

Notes. This test will return PASS without performing the exercise if an electrical-only module is installed.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Plug-In Interface Module: External 52Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 52 MHz rate. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

This test is identical to the Internal 52Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP52E

Notes. Requires user interaction.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Plug-In Interface Module: External 155Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 155 MHz rate. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

This test is identical to the Internal 155Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP155E

Notes. Requires user interaction.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

Plug-In Interface Module: External 622Mb Loop Test

This test verifies the optical data path at the 622MHz rate. The test requires user interaction to connect external loopback cables to the optical connectors.

This test is identical to the Internal 622Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP622E

Notes. Requires user interaction.

This test will return PASS without performing the exercise if an electrical-only module is installed.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page 6–88.

CPU: Vector Interrupt Test

This test verifies the processor's ability to recognize vectored interrupts. The test uses the "TESTVECTINT" bit in the Processor board Control Register to force the interrupt.

The Multi-Function Peripheral (MFP) chip is programmed to recognize the interrupt on the rising edge. The interrupt is then unmasked and enabled.

Before exiting, the interrupt is disabled and masked.

GPIB Command. DIAG:SELECT:ROUTINE CPUINT

Error Messages. Potential error messages are as follows:

Test FAIL – Unexpected Interrupt:

```
Interrupt Count Exp: 0x0, Act: 0xX
```

This message is produced if an interrupt is detected prior to forcing the interrupt. The “Act” value indicates the number of times the interrupt occurred.

Test FAIL – No Interrupt:

```
Interrupt Count Exp: 0x1, Act: 0xX
```

This message is produced if an incorrect number of interrupts occurred after forcing a single interrupt. The “Act” value indicates the number of interrupts that occurred. Typically if the test fails with this message the “Act” value will be 0, meaning the routine expected an interrupt but did not detect one.

CPU: IIC Control Test

This test verifies the processor’s ability to access the I^2C-bus controller chip. The test performs a write/read verification on the data register of the controller IC.

The test first polls the busy bit in the status register of the I^2C-bus controller chip to wait until the controller is not busy. If after a defined number of attempts the chip is still busy, the test will give up and fail.

GPIB Command. DIAG:SELECT:ROUTINE CPUIIC

Error Messages. Potential error messages are as follows:

Test FAIL – IIC Busy:

```
Addr: 0x4000000, Exp: 0x1, Act: 0x0
```

This error message is produced if the I^2C controller remains busy while the test is attempting to access the chip.

Test FAIL – IIC Access:

```
Addr: 0x4000000, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the test was unsuccessful in its attempt to modify the contents of the data register.

CPU: Clock/Calendar Test

This test verifies the functionality of the clock/calendar IC. If the test is invoked as part of the Self Test suite, the routine simply performs an access verification. Otherwise, the test also verifies the chip's 1 second interrupt.

All communication with the clock/calendar chip is via the I^2C controller chip. The test issues a set NODA (NO DAte) command and verifies the flag is set. Then the test repeats the exercise by clearing the NODA flag.

If the exercise passes and the test was not invoked as part of the Self-Test suite (which includes power-up self-test) additional verifications of the chip's ability to keep time are performed.

The test first monitors the second output to verify it is changing state. The second output should change state every 0.5 seconds. If this exercise passes the test then it verifies the 1 second interrupt. The delay loops used in the routines should be roughly 5 seconds. The tests do not verify the accuracy of the second pulse, but whether or not it is changing at all.

The routine for verifying the second interrupt is similar to the exercise described above, except the routine monitors the value of a software variable that gets updated each time the second interrupt occurs. If the variable does not change within 5 seconds the test fails (Test FAIL – Second Interrupt).

GPIB Command. DIAG:SELECT:ROUTINE CPUCLKCAL

Notes. The clock/calendar chip is an I^2C–bus component. Therefore, this test depends on the functionality of the I^2C–bus controller and circuitry.

Error Messages. Potential error messages are as follows:

Test FAIL – Set NODA:

```
Addr: 0xD0, Exp: 0x1, Act: 0x0
```

This error message is produced if the instrument was unsuccessful in its attempt to set the NODA flag within the clock/calendar chip.

Test FAIL – Reset NODA:

```
Addr: 0xD0, Exp: 0x0, Act: 0x1
```

This error message is produced if the instrument was unsuccessful in its attempt to clear the NODA flag after it was previously set.

Test FAIL – Timing:

```
Addr: 0xD0, Exp: 0x0/0x1, Act: 0x1/0x0
```

This error message is produced if the second output did not change state after monitoring for 5 seconds. The “Exp” value will either be 0 or 1 and the “Act” value will then be the opposite value.

Test FAIL – Second Interrupt:

```
Seconds Count, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the second interrupt failed to occur after a 5 second delay.

CPU: Clk/Cal Battery Test

This routine verifies the +3V battery used to power the clock/calendar IC during the instrument down time. The clock/calendar chip contains a Power Fail flag that is set if the external battery drops below the threshold value.

This test simply examines the state of the Power Fail flag in the clock/calendar chip.

GPIB Command. DIAG:SELECT:ROUTINE CPUCCBATT

Notes. The clock/calendar chip is an I^2C bus component and therefore dependent on the functionality of the I^2C bus controller IC and circuitry.

Once the power fail bit is set, the flag will remain set (even after the battery is restored) until the chip is reprogrammed.

Error Messages. Potential error messages are as follows:

Test Fail:

```
Addr: 0xD0, Exp: 0x0, Act: 0x1
```

The above error message indicates the power fail flag is set.

CPU: DUART Test

This test verifies the DUART chip. If the test is invoked as part of the Self Test suite the routine simply performs an access verification. Otherwise more thorough testing of the chip data paths and interrupts are done.

The routine is the access verification portion of the test. The test uses the Interrupt Vector Register to perform the exercise.

If the exercise passes and the test was not invoked as part of the Self-Test suite (which includes power-up self-test) additional testing is performed. These additional exercises are repeated on both channels of the DUART. If a failure is detected, the test will abort (that is, no further testing is done) and report the error.

The first extended test is the interrupt verification. The test exercises the chip in local loopback mode and verifies the Tx interrupt. The interrupt handler for the Tx interrupt places the “txData” in the transmit register then shifts “txData” left by 1. Knowing this, the test routine sets “txData” to 0x80, enables the Tx interrupt, and performs a small delay. The routine then verifies the “txData” was shifted to 0x00 by the interrupt handler.

The final extended exercise is the loopback test. This exercise verifies the DUART’s ability to transmit and receive data under interrupt control. Again, the DUART is placed in local loopback mode. The interrupt handler is responsible for the following tasks:

- Tx Side: Place “txData” in transmit register and shift “txData” left by 1. Disable Tx interrupt if “txData” is 0.
- Rx Side: Read receive register and place data in “rxData[]” array. Disable Rx interrupt if “rxData[]” is full.

GPIB Command. DIAG:SELECT:ROUTINE CPUDUART

Error Messages. Potential error messages are as follows:

Test FAIL – Access:

```
Addr: 0x500000C, Exp: 0xAA/0x55, Act: 0xXX
```

The above error message is produced if the test was unsuccessful in its attempts to access the DUART Interrupt Vector Register. The “Exp” value will either be 0xAA or 0x55.

Test FAIL – Interrupt:

```
Addr: 0x5000005, Exp: 0x1/0x10, Act: 0x0
```

The above error message is produced if the Tx interrupt failed to occur. The “Exp” value will be 0x1 for channel A and 0x10 for channel B.

Test FAIL – Loopback:

```
Addr: 0x500000F/0x500002F, Exp: 0xXX, Act: 0xXX
```

The above error message is produced if the loopback exercise failed. The “Addr” value will be 0x500000F for channel A and 0x500002F for channel B.

Display: Video RAM Test

This test verifies the display board video RAM. The test performs both a data-line- and an address-line/data pattern exercise on each of the bit-planes.

If this test is invoked as part of the self-test suite (which includes power-up self-test) the routine will use an abbreviated list of test patterns.

Each bit-plane is 1024x512 pixels (or 64 Kbytes). The graphics bit-plane uses this entire area, while the user interface planes only use the first 480 rows (or 60 Kbytes). The memory tests exercise only the portion of memory which is actually used.

GPIB Command. DIAG:SELECT:ROUTINE DISPRAM

Error Messages. For a description of the RAM Data Line Routine and possible error messages, refer to *RAM Data Line Routine* on page 6–86.

For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page 6–86.

Display: RAMDAC Test

This test verifies the color palette memory of the RAM DAC. The test performs a simple data pattern exercise.

GPIB Command. DIAG:SELECT:ROUTINE DISPDAC

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Addr: 0x990001, Exp: 0xXX, Act: 0xXX
```

Display: White Field Test

This test fills the screen with a solid high–intensity pattern. The test requires user interaction to verify the screen is filled with a uniform intensity.

This test programs the RAM DAC to produce 100% intensity output, then updates the appropriate video bit-plane with a solid filled box.

GPIB Command. DIAG:SELECT:ROUTINE DISPWF

Notes. Requires user interaction.

Error Messages. None.

Display: Grey Field Test

This test fills the screen with a solid medium-intensity pattern. The test requires user interaction to verify the screen is filled with a uniform intensity of the appropriate level.

This test programs the RAM DAC to produce 30% intensity output, then updates the appropriate video bit-plane with a solid filled box.

GPIB Command. DIAG:SELECT:ROUTINE DISPGF

Notes. Requires user interaction.

Error Messages. None.

Display: White Box Test

This test draws two solid boxes, one high–intensity box centered within a longer medium intensity box. The test is useful for visually comparing the contrast in intensity levels.

GPIB Command. DIAG:SELECT:ROUTINE DISPWB

Notes. Requires user interaction.

Error Messages. None.

Display: Test Grid Test

This test draws a test grid on the screen. The test is useful for determining if the display is properly centered.

GPIB Command. DIAG:SELECT:ROUTINE DISPTG

Notes. Requires user interaction.

Error Messages. None.

Display: Composite Test

This test draws a test grid along with various line–filled boxes of differing orientation. The test is useful for identifying geometric distortions in the CRT.

GPIB Command. DIAG:SELECT:ROUTINE DISPCOMP

Notes. Requires user interaction.

Error Messages. None.

Display: HW Scrolling Test

This test exercises the hardware scrolling machinery. The test requires user interaction to verify that the scrolling checkerboard pattern scans completely and smoothly (no jumps) in both the horizontal and vertical direction.

GPIB Command. DIAG:SELECT:ROUTINE DISPSCROLL

Notes. Requires user interaction.

Error Messages. None.

Front Panel General Notes

The processor communicates with the front panel using the A Channel of the MC68681 DUART (located on the processor board). All diagnostics are done with the interrupts disabled. The software polls the hardware to determine the status of the transmitter/receiver when sending/receiving bytes. This polling method has an associated timeout. If the hardware does not respond within the allotted time, the test fails and produces one of the error messages described in the following *Front Panel Error Messages* section.

In transitioning from an interrupt-driven to a polling method of controlling the communication hardware, the routine needs to send a dummy command to the Front Panel after disabling the interrupts. This dummy command is performed as the first step in all of the Front Panel tests. The op-code of this NOP command is:

Front Panel NOP Command: 0xC0

When the instrument is first powered on, the host processor and the front panel processor perform an initialization sequence to properly recognize and configure the hardware. During this hardware initialization phase if a failure is detected the Self-Test diagnostics will report one of the error messages described in the following *Front Panel Error Messages* section.

Front Panel Error Messages

Test FAIL – Sending Bytes To Front Panel:

```
Time-Out Sending All Bytes, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the front panel is not ready to receive the next byte of a command within a reasonable amount of time. The “Exp” value contains the number of bytes in the command the software was attempting to send. The “Act” value contains the actual number of bytes successfully sent.

Test FAIL – Receiving Bytes From Front Panel:

```
Time-Out Reading All Bytes, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the DUART does not receive the next byte of a response from the front panel within a reasonable amount of time. The “Exp” value contains the number of bytes in the response the software was expecting to receive. The “Act” value contains the actual number of bytes successfully read.

Test FAIL – Self-Test Status:

```
Front Panel Status Byte, Exp: 0xE0, Act: 0xXX
```

The first byte after power-up reported by the front panel processor is the status of its internal self-test. The “Exp” field contains the expected status while the “Act” field contains the actual results.

Test FAIL – Self-Test Communication:

```
Front Panel Data Byte, Exp: 0xXX, Act: 0xXX
```

If the front panel passes its internal self-test, the two processors will then attempt to verify the communication path by having the host processor send the following sequence of bytes to the front panel which simply echoes the characters back:

```
0xA5, 0x4B, 0x96, 0x2D
```

The error message shown above is produced if the bytes received do not match the bytes sent.

Front Panel: Internal Test

This test instructs the front panel processor to perform its internal self-test and report back the results.

GPIB Command. DIAG:SELECT:ROUTINE FPINT

Notes. Refer to *Front Panel General Notes* on page 6–126 for a description of other possible failure modes relating to front panel communication.

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Status Byte Contains Error, Exp: 0xE0, Act: 0xXX
```

The “Exp” field contains the expected status for No Failures, while the “Act” field contains the actual self-test status reported by the front panel processor.

Front Panel: LEDs Test

This test exercises each of the front panel LEDs. Although the front panel processor contains a LED test that can be invoked on demand, the order in which the LEDs are lighted is hard to follow. Therefore, the LEDs are explicitly controlled by the host processor.

This test requires user interaction to verify the LEDs light in the correct order and that only one LED is lighted at a time. Skipping over LEDs or lighting multiple LEDs simultaneously would be considered a failure.

The test exercises the set of front panel LEDs in the following order:

YELLOW LEDs	(Starting at top of the left column)
RED LEDs	(Starting at top of the left column)
GREEN LEDs	(Starting with status LEDs, then lighting top row of functions LEDs right to left)

This test uses two separate front panel LED commands. The first form turns on/off a single LED. The second form requires two LED IDs, and turns the first LED off and the second one on.

GPIB Command. DIAG:SELECT:ROUTINE FPLEDS

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page 6–126 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Front Panel: Speaker Test

This test instructs the front panel to "ring" the bell. The test requires user interaction to verify the bell does indeed make the appropriate sound.

GPIB Command. DIAG:SELECT:ROUTINE FPSPKR

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page 6–126 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Front Panel: Manual Test

This test provides an interactive verification of the front panel buttons and knob. The test requires user interaction and provides visual feedback of button presses and knob turns.

GPIB Command. DIAG:SELECT:ROUTINE FPINTR

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page 6–126 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Disk: PM110 Register Test

This test verifies the processor's ability to access the internal registers of the PM110 ASIC by performing a walking 1's exercise on various registers.

GPIB Command. DIAG:SELECT:ROUTINE DISKREG

Error Messages. For a description of the RAM Data Line Routine and possible error messages, refer to *RAM Data Line Routine* on page 6–86.

The RAM Data Line exercise performed is for byte wide memory.

Disk: PM110 Cache Test

This test verifies the integrity of the PM110 cache memory by performing an address line/data pattern exercise on the entire memory range.

GPIB Command. DIAG:SELECT:ROUTINE DISKCACHE

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page 6–86.

The RAM Address Line/Data Pattern exercise is for byte-wide memory.

Disk: PM110 Counter Test

This test verifies the internal counters of the DMA portion of the PM110. The exercise manually increments the counters and verifies the terminal count status responds at the correct location.

GPIB Command. DIAG:SELECT:ROUTINE DISKCNTR

Error Messages. Test FAIL – Terminate Early:

The following error message is produced if the terminal count status is high before the counter reaches the end count. The "Act" field contains the count value when the status went high.

```
Addr: 0x980001, Exp: 0x0, Act: 0xX
```

Test FAIL – No Termination:

The following error message is produced if the terminal count status fails to go high after the counter expires.

```
Addr: 0x980001, Exp: 0x0, Act: 0x0
```

Disk: Controller Test

This test initializes the DP8473 Floppy Disk Controller and verifies "No Errors" were reported.

GPIB Command. DIAG:SELECT:ROUTINE DISKCONT

Error Messages. Potential error messages are as follows:

Test Fail:

```
Unable to Initialize dp8473, Exp: 0x1, Act: 0x0
```

The above error message indicates the routine used to initialize the Floppy Disk Controller returned with an error status.

Disk: Drive Test

This test verifies the floppy disk drive responds properly when initialized.

GPIB Command. DIAG:SELECT:ROUTINE DISKDRV

Notes. Since the floppy drive plastic bezel can warp if subjected to the cycle room, the floppy is not installed during cycle room testing. The test reads protocol board DIP switch 3 as an indicator the drive is not installed. If the switch is set, the test simply returns PASSED without attempting to access the missing hardware.

Error Messages. Potential error messages are as follows:

Test FAIL – Disk Controller:

```
dp8473 not initialized, Exp: 0x1, Act: 0x0
```

The above error message indicates the routine used to initialize the Floppy Disk Controller returned with an error status.

Test FAIL – Disk Drive:

```
Unable to Init Floppy Drive, Exp: 0x1, Act: 0x0
```

The above error message indicates the routine used to initialize the Floppy Drive returned with an error status.

Disk: Format & Verify Test

This test verifies the ability to properly format and label a disk. The test requires user interaction to insert a disk in the drive before invoking the test.

GPIB Command. DIAG:SELECT:ROUTINE DISKFNV

Notes. Requires user interaction.

This test erases the contents of the disk.

Error Messages. Potential error messages are as follows:

Test FAIL – File Open:

The following error message is produced if the test fails to gain access to the disk for performing disk operations.

```
Unable to open "fd0:/", Exp: 0x1, Act: 0x0
```

Test FAIL – Format:

The following error message is produced if the disk FORMAT operation reports an error status.

```
Unable to format floppy disk, Exp: 0x1, Act: 0x0
```

Test FAIL – Init:

The following error message is produced if the disk INITIALIZE operation reports an error status.

```
Unable to init floppy disk, Exp: 0x1, Act: 0x0
```

Test FAIL – Label:

The following error message is produced if the disk LABEL operation reports an error status.

```
Unable to Label floppy disk, Exp: 0x1, Act: 0x0
```

Test FAIL – File Close:

The following error message is produced if the test fails to close the file upon completion of the test.

```
Unable to close floppy disk, Exp: 0x1, Act: 0x0
```

Disk: Dysan Seek Test

This test requires a special Dysan disk (DDD 305–400 P/N 810244) to perform the exercise. The test reads selected tracks using both heads to check for a specified pattern on the disk. If any of the tracks fail, the test fails.

The test requires user interaction to insert the Dysan disk into the drive prior to invoking the test.

GPIB Command. DIAG:SELECT:ROUTINE DISKSEEK

Notes. Requires user interaction.

Error Messages. Potential error messages are as follows:

Test FAIL – Disk Drive:

The following error message indicates the routine used to initialize the Floppy Drive returned with an error status.

```
Floppy Drive Not Initialized, Exp: 0x1, Act: 0x0
```

Test FAIL – Disk Read:

The following error message is produced if the test fails when attempting to read the Dysan ID string.

```
Unable to Read Dysan Disk, Exp: 0x1, Act: 0x0
```

Test FAIL – Dysan ID:

The following error message is produced if the Dysan ID string read from the disk is not as expected.

```
Incorrect ID for Dysan Disk, Exp: 0x1, Act: 0x0
```

Test FAIL – Sector Read:

Once inside the test loop of examining specific locations on the disk, the following error message will be produced if the test reads an unexpected number of bytes from the disk.

```
Incorrect number of bytes read from disk,
             Exp: 0x1, Act: 0x0
```

Test FAIL – Sector ID:

Once inside the test loop of examining specific locations on the disk, the following error message will be produced if the test reads an incorrect ID string from the disk.

```
Incorrect id read from disk, Exp: 0x1, Act: 0x0
```

Tributary General Notes

This section describes tests you can use to troubleshoot the tributary circuitry, For each test, this section gives a brief description of the test, its GPIB command, and possible error messages.

Tributary: Trib Flash Voltage Test

This test checks for the flash ROM program voltage enabled.

The voltage level of the program voltage is read through the status register and indicates when +12 V is applied to the flash ROM.

GPIB Command. DIAG:SELECT:ROUTINE TRIBVFL

Notes. Accessed by initiating the complete tributary diagnostics.

Error Messages. Potential error messages are as follows:

Test FAIL:

```
"Tributary Flash VPP Voltage is ON"
```

Tributary: Trib Flash Checksum Test

This test verifies the integrity of the tributary board flash EEPROM device using a standard checksum routine.

The checksum routine used is a simple 16-bit summation. The routine reads a 16-bit value from memory and adds it to a running checksum.

GPIB Command. DIAG:SELECT:ROUTINE TRIBCKSUM

Notes. Accessed by initiating the complete tributary diagnostics.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the calculated checksum (“Act”) does not match the value stored in memory (“Exp”).

```
Addr: 0xA8000C, Exp: 0xX, Act: 0xX
```

Tributary: DSn Test Set

This test verifies the ability of the tributary hardware to generate and receive DSn alarms, errors, framing formats, and patterns. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

These tests are the basic building blocks of all tributary diagnostics. Therefore, if these tests fail then the rest of the tributary diagnostics will also fail.

This routine calls the standard DSn test set tests to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1TS
DIAG:SELECT:ROUTINE TRIBDS3TS

Notes. None.

Error Messages. See *diagGroupTestSet (Tributary Rate)*, on page 6–90, for a list of possible error messages.

Tributary: En Test Set

This test verifies the ability of the tributary hardware to generate and receive En alarms, errors, framing formats, and patterns. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

These tests are the basic building blocks of all tributary diagnostics. Therefore, if these tests fail then the rest of the tributary diagnostics will also fail.

This routine calls the standard En test set tests to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1TS
DIAG:SELECT:ROUTINE TRIBE3TS

Notes. None.

Error Messages. See diagGroupTestSet (Tributary Rate), on page 6–90, for a list of possible error messages.

Tributary: Register Access

This test verifies the ability of the processor to access all tributary board registers. The test provides a quick verification that the board is alive and that various components can be programmed.

The test is modeled after the standard RAM address-line/data pattern routine. Each register requires a mask value as not all bits are R/W and some bits affect other registers.

GPIB Command. DIAG:SELECT:ROUTINE TRIBREG

Notes. This test is destructive to the state of the tributary hardware and therefore re–initializes the Tributary board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the routine fails. The “Addr” field contains the address of the register that failed.

```
Addr: 0xX, Exp: 0xX, Act: 0xX
```

Tributary: DSn Line Interface (External Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx external loopback path at the DSn line interface. An external cable is required at the DSn connectors to run this test.

This routine calls the standard DSn line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1LIFE
DIAG:SELECT:ROUTINE TRIBDS3LIFE

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page 6–93, for a list of possible error messages.

Tributary: En Line Interface (External Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx external loopback path at the En line interface. An external cable is required at the En connectors to run this test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1LIFE
DIAG:SELECT:ROUTINE TRIBE3LIFE
DIAG:SELECT:ROUTINE TRIBE4LIFE

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page 6–93, for a list of possible error messages.

Tributary: DSn Line Interface (Internal Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx loopback path at the DSn line interface. An external cable is not required at the DSn connectors to run this test.

This routine calls the standard DSn line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1LIFI
DIAG:SELECT:ROUTINE TRIBDS3LIFI

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page 6–93, for a list of possible error messages.

Tributary: En Line Interface (Internal Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx loopback path at the En line interface. An external cable is not required at the En connectors to run this test.

This routine calls the standard En line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1LIFI
DIAG:SELECT:ROUTINE TRIBE3LIFI
DIAG:SELECT:ROUTINE TRIBE4LIFI

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page 6–93, for a list of possible error messages.

Tributary: DSn Mapper/Demapper

This test verifies the ability of the tributary hardware to generate and receive VT failures, alarms, errors, background patterns, and background framing formats. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

This routine calls the standard DSn mapper/demapper tests.

GPIB Command. DIAG:SELECT:ROUTINE TRIBVTMAP
DIAG:SELECT:ROUTINE TRIBDS3MAP

Notes. None.

Error Messages. See the *diagGroupMapDemap (Tributary Rate)*, on page 6–94, for a list of possible error messages.

Tributary: En Mapper/Demapper

This test verifies the ability of the tributary hardware to generate and receive TU failures, alarms, errors, background patterns, and background framing formats. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

This routine calls the standard En mapper/demapper tests.

GPIB Command. DIAG:SELECT:ROUTINE TRIBTU12MAP
DIAG:SELECT:ROUTINE TRIBTU3MAP
DIAG:SELECT:ROUTINE TRIBE4MAP

Notes. None.

Error Messages. See the *diagGroupMapDemap (Tributary Rate)*, on page 6–94, for a list of possible error messages.

Tributary: DSn Ring

This test verifies the overall operation of the Tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various VT and DSn alarms, errors, and failures are tested.

Ring Configuration: (Test Set (Tx) –> (Rx) Mapper/Demapper (Tx)
–> (Rx) Line Interface (Tx) –> (Rx) Test Set)

This test should be run after all the other tributary tests have passed.

This routine calls the standard DSn ring test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1RING
DIAG:SELECT:ROUTINE TRIBDS3RING

Notes. None.

Error Messages. See the *diagTribRing(Tributary Rate)*, on page 6–97, for a list of possible error messages.

Tributary: En Ring

This test verifies the overall operation of the Tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various TU and En alarms, errors, and failures are tested.

Ring Configuration: (Test Set (Tx) –> (Rx) Mapper/Demapper (Tx)
–> (Rx) Line Interface (Tx) –> (Rx) Test Set)

This test should be run after all the other tributary tests pass.

This routine calls the standard En ring test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1RING
DIAG:SELECT:ROUTINE TRIBE3RING

Notes. None.

Error Messages. See the *diagTribRing(Tributary Rate)*, on page 6–97, for a list of possible error messages.

Jitter/Wander General Notes

This section describes tests you can use to troubleshoot the jitter/wander generation and measurement circuitry, For each test, this section gives a brief description of the test, its GPIB command, and possible error messages.

JAWA: Clock Recovery Circuit

This test verifies the operation of the JAWA clock recovery circuit. There is a separate test for each rate. The 155 Mb/s test also tests the 140 Mb/s rate.

GPIB Commands. DIAG:SELECT:ROUTINE JMEACR2M
DIAG:SELECT:ROUTINE JMEACR34M
DIAG:SELECT:ROUTINE JMEACR155M
DIAG:SELECT:ROUTINE JMEACR52M
DIAG:SELECT:ROUTINE JMEACR622M

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the clock recovery circuit cannot be disabled (in this error message, the data xxx is meaningless):

`CRC undisable, Exp: xxx, Act: xxx`

The following error message is produced if the clock recovery circuit cannot be enabled (in this error message, the data xxx is meaningless):

`CRC unenable, Exp: xxx, Act: xxx`

The following error message is produced if the oscillator will not tune over the proper frequency range:

<data rate>`, Exp:` <limit frequency>`, Act:` <measured frequency>

The following error message is produced if the oscillator will not synchronize:

<data rate>`, Exp:` <expected frequency>`, Act:` <measured frequency>

JAWA: Register Access

This test verifies the registers on the JAWA and JAWG boards.

GPIB Command. DIAG:SELECT:ROUTINE JITREG

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the test fails:

`Addr:` <register address>`, Exp:` <value written>`, Act:` <value read>

JAWA: Flash Memory Checksum

This test verifies the JAWA EEPROM using a checksum algorithm.

GPIB Command. DIAG:SELECT:ROUTINE JMEACKSUM

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the proper flash memory header is not read:

`Addr:` <start address of flash>`, Exp: 0xc3a5, Act:` <ID read>

The following error message is produced if the calculated checksum does not match the value stored in memory:

`Addr:` <start address of checksum>`, Exp:` <calculated>`, Act:` <read from flash>

JAWA: DAC Loopback

This test verifies the multiple-output DAC on the JAWA board.

GPIB Command. DIAG:SELECT:ROUTINE JITDACLB

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read value does not match the written value to within a specific tolerance:

`Addr: 0xb1a018, Exp:` <value written>`, Act:` <value read>

JAWA: Clock Recovery Divider

This test verifies the function of the clock recovery divider.

GPIB Command. DIAG:SELECT:ROUTINE JMEADIVA

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if two computed frequencies do not match:

`freq diff<100kHz, Exp: 0x186a0, Act:` <difference between computed frequencies>

JAWA: Tracking PLL

This test verifies the function of the tracking phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEATRL

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop fails to lock:

`freq diff<thresh, Exp: 0x186a0, Act:` <measured frequency difference>

The following error message is produced if the loop fails to unlock when it should:

`can't unlock, Exp:` <frequency limit (max)>`, Act:` <measured frequency>

JAWA: Measurement Phase Detector

This test verifies the function of the phase detector in the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPLPHDET

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop amplitude is correct (reference amplitude is measured with 1.3 MHz filter):

`Minimum:` <40% of reference amplitude>`, Maximum:` <60% of reference amplitude>`, Actual:` <measured value with 400 kHz filter>

JAWA: Measurement PLL Locking

This test verifies the function of the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPLOCK

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop does not lock:

```
PLL can't lock, Exp: 0x0, Act: 0x1
```

JAWA: Measurement PLL Gain

This test verifies the function of the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPGAIN

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop does not lock:

`VGA Fail@STM1E, Exp: 0x2, Act:` <measured gain ratio>

JAWA: FIFO

This test verifies that the FIFO can be written and read.

GPIB Command. DIAG:SELECT:ROUTINE JMEAFIFO

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the FIFO reports full immediately after being reset:

```
FIFO Active Stuck High, Exp: 0x0, Act: 0x1
```

The following error message is produced if the value written to the FIFO does not match the value read back from it:

`Addr:` <offset in FIFO of difference>`, Exp:` <value written>`, Act:` <value read>

JAWA: Analog Output

This test verifies that the path between jitter generation and jitter measurement is working.

GPIB Command. DIAG:SELECT:ROUTINE JMEAAOUT

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the analog output calibration fails:

`A out cal failed, Exp: 0x0, Act: 0x0`

The following error message is produced if the proper frequency is not measured at the analog output:

<data rate>`, Exp:` <expected frequency>`, Act:` <measured frequency>

JAWG: Wander Loop Locking

This test verifies phase locked loop that is used to generate wander. The test checks that the loop is initially locked, that it will unlock on command, and reacquire a lock on command.

GPIB Command. DIAG:SELECT:ROUTINE JGENWLLOCK

Error Messages. Potential error messages are as follows:

The following error message is produced if the PLL will not lock:

`wander loop unlock, Exp: 0x63, Act:` <measured frequency difference>

The following error message is produced if the PLL will not unlock:

`wander loop not unlock, Exp:` <VCO frequency limit>`, Act:` <measured frequency difference>

JAWG: Jitter Loop Locking

This test verifies phase locked loop that is used to generate jitter. The test checks that the loop locks for all rates and ranges and that the loop is not oscillating.

GPIB Command. DIAG:SELECT:ROUTINE JGENJLLOCK

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

<data rate> <range> `UI cal fail, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

<data rate> <range> `UI lock fail, Exp: 0x1, Act: 0x0`

JAWG: Jitter Loop Low-Pass Filters

This test verifies the selectable low-pass filters in the jitter generator phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JGENJLPF

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

<filter bandwidth> `cal fail, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

<filter bandwidth> `lock fail, Exp: 0x1, Act: 0x0`

JAWG: Jitter Generation

This test verifies that the JAWG hardware is producing jitter.

GPIB Command. DIAG:SELECT:ROUTINE JGENFUNC

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

`JGEN loop offset won't cal, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

`JGEN loop unlock@STM1E, Exp: 0x1, Act: 0x0`

The following error message is produced if the peak amplitude reading is too low to indicate jitter:

`peak det low@STM1E, Exp: 0x1f4, Act:` <peak reading>

Notes. The test does not rely on the jitter measurement hardware.

Troubleshooting Sequence

The Troubleshooting Sequence allows qualified technicians to determine which board in a CTS instrument to replace. You use the results of the CTS Diagnostics to make this determination. The troubleshooting sequence assumes that you are familiar with the CTS Diagnostic System and its use.

The troubleshooting sequence is shown in Table 6–16 on page 6–146. After running the diagnostics, compare the results with the Diagnostic Test Results column of the table. Follow the procedure for the lowest numbered step where the Diagnostic Test Results match your results when running the diagnostics.

The test numbers, shown in Tables 6–13 through 6–15 on page 6–101, are the test numbers associated with each diagnostic. These numbers are displayed with the diagnostic results in the Error Log.

The Error Log is a history of all the diagnostic tests that have been executed since the last time the log was cleared. The Error Log can be accessed as follows:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	VIEW RESULTS	Page Up (5 times)
		VIEW RESULTS	Error Log

If the problem is occurring regularly, it may be useful to clear the Error Log and then run the diagnostics so that the present error results are easy to see. To clear the Error Log:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	VIEW RESULTS	Clear
		VIEW RESULTS	Exit

If the problem is intermittent, look at the last entry in the Error Log. Use the Page Down selection to move to the last entry in the Error Log. If the Error Log becomes full, the first entry in the Log (the oldest data) is discarded.

Table 6–16: Troubleshooting Sequence

Step	Diagnostic Test Results	Procedure
1.	BUS FAULT @ 0X9B05XX OR 0X9B0AXX INTERNAL ERROR 1 (SYSTEM EVENT 6) NO OUTPUT FROM CPU RS232 PORT	This combination of failures indicates that the +12 V or –12 V power supply generated by the Backplane board is faulty. Use the Backplane Troubleshooting Procedure to isolate the problem.
2.	No output from CPU RS232 port No +12 V present on U39 pin 1 and U38 pin 1 on the CPU board No –12 V present on U39 pin 8 and U38 pin 8 on the CPU board	This special case is caused by the lack of +12 V and/or –12 V on the RS232 interface chips, U38 and U39. Use the Backplane Troubleshooting procedure to isolate the problem.
3.	No output from CPU RS232 port +12 V present on U39 pin 1 and U38 pin 1 on the CPU board –12 V present on U39 pin 8 and U38 pin 8 on the CPU board	A failure of the RS232 output has the following possible causes(in order of probability): 1. CPU board 2. Cable from CPU board to RS232 output connector
4.	CPU tests except Clk/Cal Battery (1, 2, 3, and 5) fail	Failure of any CPU or Processor Diagnostic indicates a failure on the CPU board. The CPU board should be replaced before any other troubleshooting is attempted.
5.	Clk/Cal Battery (4) failure	The most likely cause of a Clk/Cal Battery failure is the Back-Up battery, the cable or connectors from the battery to the CPU board, or the battery has been disconnected and then connected (it could be an intermittent cable). If you know that the battery has been disconnected and then reconnected, then use UTILITY/MISC SETTINGS to set the time and date. After the time and date have been set, power the instrument OFF and then ON. The Clk/Cal Battery failure should not appear. If the failure still appears, replace the CPU board. If the condition of the battery or cable is suspect, replace them, and then set the time and date. After the time and date have been set, power the instrument OFF and then ON. The Clk/Cal Battery failure should not appear. If the failure still appears, replace the CPU board.
6.	Bus fault @ 0x9b05XX or 0x9b0AXX	A bus fault on the ITX(0x9b05XX) or the Hardware Timer (0x9b0AXX) indicates the Tx clock is not present in the system. The Tx Clock gets to the Protocol system from the Clock board. The lack of a Tx clock can be caused by the following items (in order of probability): 1. Cable from Clock board to Main Protocol board 2. High Speed Protocol board 3. Clock board 4. Main Protocol board

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
7.	Internal error 1 (System Event 6)	This fault is caused by the SETI chip on the High Speed Protocol board not being able to lock to the SETI_REFCLK clock signal. The fault can be caused by the following items (in order of probability): 1. Cable from Clock Board to Main Protocol Board 2. High Speed Protocol board 3. Clock board 4. Main Protocol board
8.	Bus fault @ 0x9b06XX	This failure indicates a problem with the clock for the Rx portion of the Protocol system. The fault can be caused by the following items (in order of probability): 1. If failure is on 52 Mb/s data rate, Plug-In Interface Module 2. High Speed Protocol board 3. Main Protocol board
9.	Any clock board diagnostic fails	This failure indicates a problem with the Clock board circuitry. The fault can be caused by the following items (in order of probability): 1. Clock board 2. Backplane board (low probability) 3. CPU board (low probability)
10.	Bus fault @ 0x9b05XX or 0x9b0AXX Any clock board diagnostic fails	These failures indicate the following possible causes (in order of probability): 1. Clock Board 2. Cable from Clock board to Main Protocol board 3. High Speed Protocol board 4. Main Protocol board
11.	Internal error 1 (System Event 6) Any clock board diagnostic fails	These failures indicate the following possible causes (in order of probability): 1. Clock board 2. Cable from Clock board to Main Protocol board 3. High Speed Protocol board 4. Main Protocol board
12.	Plug-In Interface Module status fails	The system does not detect that a Plug-In Interface Module is installed. The fault can be caused by the following items (in order of probability): 1. Plug-In Interface Module 2. Main Protocol board
13.	Plug-In Interface Module identification (42) fails Plug-In Interface Module access (43) passes	This indicates a failure to read the O/E Identification Register and yet the Plug-In Interface Module Access test passed. The fault is caused by the Plug-In Interface Module.
14.	Plug-In Interface Module identification (42) passes Plug-In Interface Module access (43) fails	This indicates a failure to read and/or write to the Plug-In Interface Module. This indicates a failure to read the O/E Identification Register. The fault is caused by the Plug-In Interface Module.

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
15.	Plug-In Interface Module identification (42) fails Plug-In Interface Module access (43) fails	This indicates a failure to read the O/E Identification Register and a failure to access the Plug-In Interface Module registers. The fault can be caused by the following items (in order of probability): 1. Plug-In Interface Module 2. 100 pin cable from Display board to Main Protocol board 3. Main Protocol board 4. Backplane board 5. Display board 6. CPU board
16.	Plug-In Interface Module Tx optical power (44) fails Protocol board A/D converter (34) passes	This indicates a failure to obtain a voltage from the Plug-In Interface Module that is within the expected range for the Tx optical power. The fault can be caused by the following items(in order of probability): 1. Plug-In Interface Module 2. Main Protocol board
17.	Protocol board A/D converter (34) fails	This indicates a failure of the A/D converter on the Main Protocol board to correctly measure the GND and 2.5 V reference signals. The fault is caused by the Main Protocol board.
18.	Protocol board A/D converter (34) passes Plug-In Interface Module Rx optical power (45) fails	This indicates a failure to obtain a voltage from the Plug-In Interface Module that is within the expected range for the Rx optical power. The fault can be caused by the following items (in order of probability): 1. No cable attached for External Loopback 1. Plug-In Interface Module 2. Main Protocol board
19.	Any Display board diagnostics fail	This indicates a failure in the Display board circuitry. The fault can be caused by the following items (in order of probability): 1. Display board 2. Backplane board (low probability) 3. CPU board (low probability)
20.	Any Front Panel diagnostics	This indicates a failure in the Front Panel system. The fault can be caused by the following items (in order of probability): 1. Front Panel board 2. Cable from Front Panel board to CPU board 3. CPU board (very low probability)
21.	Any Display board diagnostics pass Disk Drive diagnostics (14, 15, 16, or 17) fail	These failures indicate a problem with the disk drive electronics. The fault is caused by the Display board.

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
22.	Any Display board diagnostics pass Disk Drive diagnostics (14, 15, 16, or 17) pass Disk Drive diagnostics (18, 19, or 20) fail	These failures indicate a problem with the physical disk drive. The fault can be caused by the following items (in order of probability): 1. Cable from disk drive to display board 2. Disk drive 3. Display board
23.	Internal error 2 or 3 (system event 7 or 8)	These errors indicate the software system was not able to detect the presence of the Main Protocol board. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. Display board (low probability) 4. Backplane board (low probability) 5. CPU board (low probability)
24.	Internal event 4 (system event 14)	This error message indicates an error was detected while communicating with the Plug-In Interface Module over the I^2C bus. A better definition of the problem can probably be found by running the Plug-In Interface Module diagnostics #41, #42, and #43 since each of these diagnostics use the I^2C bus to communicate with the Plug-In Interface Module.
25.	Misc Reg (25) fails	This failure indicates a problem writing and/or reading data from the MISC register on the Main Protocol board. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. Display board (low probability) 4. Backplane board (low probability) 5. CPU board (low probability)
26.	Misc Reg (25) passes Register access (27) fails	This failure indicates a problem writing or reading data from a number of different registers on the Main and High Speed Protocol boards. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. High Speed Protocol board 4. Display board (low probability) 5. Backplane board (low probability) 6. CPU board (low probability)

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
27.	FLASH voltage	This indicates the FLASH programming voltage has been left enabled on the Display board. The fault can be caused by the following items (in order of probability): 1. Protocol board Programming Enable switch on the Display board is left in ON position 2. Cable from Display board to Main Protocol board 3. Main Protocol board 4. Display board (low probability)
28.	Register access (27) passes FLASH checksum (29) fails	This indicates the checksum calculated for the FLASH on the Main Protocol board does not agree with the checksum stored in the FLASH. The fault can be caused by the following items (in order of probability): 1. Main Protocol board 2. Display board (low probability)
29.	Register access (27) passes ITX RAM (30) fails	This indicates a failure occurred while trying to write and/or read the ITX RAM on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
30.	Register access (27) passes IRX RAM (31) fails	This indicates a failure occurred while trying to write and/or read the IRX RAM on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
31.	Register access (27) passes PRX RAM (32) fails	This indicates a failure occurred while trying to write and/or read the PRX RAM on the Main Protocol board. The fault is caused by the Main Protocol board.
32.	Register access (27) passes IRX RAM (31) passes IRX FIFO (33) fails	This indicates a failure occurred while trying to write and/or read the IRX FIFO on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
33.	Power supply (33) fails	This indicates that one or more of the power supplies generated on the Main Protocol board is not at its expected voltage. The fault can be caused by the following items (in order of probability): 1. Plug-In Interface Module 2. High Speed Protocol board 3. Main Protocol board 4. Low Voltage Power Supply
34.	Protocol board 52, 155, 622 Mb/s loop (36, 37, and 38) passes Plug-In Interface Module 52, 155, 622 Mb/s internal loop (46, 47, or 48) fails	This indicates one or more failures were detected when looping the Tx signal back to the Rx, within the Plug-In Interface Module. These faults can be caused by the following items (in order of probability): 1. Plug-In Interface Module 2. High Speed Protocol board 3. Main Protocol board (low probability)

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
35.	Protocol board 52, 155, 622 Mb/s loop (36, 37, and 38) passes Plug-In Interface Module 52, 155, 622 Mb/s internal loop (46, 47, and 48) passes Plug-In Interface Module 52, 155, 622 Mb/s external loop (49, 50, and 51) fails	This indicates one or more failures were detected when looping the Tx signal back to the Rx through external cables. These faults can be caused by the following items (in order of probability): 1. External cables not attached or not connected properly 2. If the failures only involve Optical signals, the problem may be dirty optical cables or connectors 3. Plug-In Interface Module 4. Main Protocol board (low probability)
36.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails with B1 and/or B2 errors detected but not inserted	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol Board. These faults can be caused by the following items (in order of probability): 1. High Speed Protocol board 2. Main Protocol board 3. Clock Generator board
37.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Fails with B3 errors detected when not inserted	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol Board. Since there are B3 errors but no B1 and/or B2 errors, the following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board (low probability) 3. Clock Generator board (low probability)
38.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Fails with Pattern Loss detected	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since there are no B3 errors but there is a Pattern Loss, the problem is most likely in the Path processing on the Main Protocol board. If, however, there is only a single occurrence of a Loss of Pattern when the system is allowed to loop on diagnostics for several hundred passes, then the most likely failure is the frame pulse generated from the STTX on the High Speed Protocol board. This is a failure mode that is only activated by the diagnostic loop and causes no problem in normal operation. This single occurrence failure should be ignored and no repair attempted. If the problem is persistent Loss of Pattern, then the following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
39.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Does not fail with Pattern Loss detected Fails with B1 and/or B2 errors inserted but not detected	This indicates the diagnostics tried to insert errors, but no errors were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since the diagnostics stop when finding a B1 or B2 error, the condition of the B3 error insertion is unknown. But since no other problems were found with the B1 and/or B2 functions, it is more likely that the problem is with the error insertion function which is done through the Hardware Timer module on the Main Protocol board. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
40.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Does not fail with Pattern Loss detected Does not fails with B1 and/or B2 errors inserted but not detected Fails with B3 errors inserted but not detected	This indicates the diagnostics tried to insert errors, but no errors were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since problems were found only in the B3 error function, the Main Protocol board is the most likely candidate since all B3 error insertion functions are on the Main Protocol board. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
41.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Does not fail with Pattern Loss detected Does not fail with B1 and/or B2 errors inserted but not detected Does not fail with B3 errors inserted but not detected Fails positive and/or negative pointer movements	Since all Pointer Processing functions for the Protocol Board diagnostics are on the Main Protocol board, the Main Protocol board is the most likely cause of the problem. The following items (in order of probability) should be checked: 1. Main Protocol board 2. Clock Generator board (low probability)
42.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails STS-3/OC-3/OC-12 only with STS-3c structure	The diagnostics tests STS-3, OC-3, and OC-12 operation with both STS-1 and STS-3c structure. If problems are found only in STS-3c structure, the most likely cause is the Main Protocol board which generates the Path level information. The problem can also be in the High Speed Protocol board where the Path level clock signal originates. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)

Table 6–16: Troubleshooting Sequence (Cont.)

Step	Diagnostic Test Results	Procedure
43.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails with LOS and/or LOF detected	This failure indicates that an LOS or LOF failure was detected at some time during the diagnostic when it was not expected. The following items (in order of probability) should be checked: 1. High Speed Protocol board 2. Main Protocol board (low probability) 3. Clock Generator board (low probability)
44.	JAWA/JAWG Option 14 is installed but not recognized by the CTS 750. The message "Jitter/Wander Option Not Installed" is displayed.	Verify correct connection of all cables to the JAWA/JAWG assembly, in particular, the short coaxial cable to the Clock Generator board.
45.	Jitter fails to calibrate at STM0.	Verify that the two cables from the JAWA/JAWG assembly to the Protocol board are installed correctly.
46.	Jitter fails to calibrate at one of the tributary rates.	Verify that the cables from the JAWA/JAWG assembly to the Tributary assembly are installed correctly. The following items (in order of probability) should be checked: 1. Tributary Assembly
47.	JAWA/JAWG diagnostic codes fail (78 through 97)	Verify correct connection of all cables to the JAWA/JAWG assembly. The following items (in order of probability) should be checked: 1. JAWA/JAWG assembly 2. Tributary Assembly 3. Clock Generator board

An Example of Fault Isolation

The following results were obtained from running the System External and System Internal diagnostics.

After running the System External diagnostics:

```
O/E Ext 155 Mb Loop Elec 155 Mb
            LOS Exp:0x0 Act:0x1

O/E Ext 622 Mb Loop Opt 622 Mb
            LOS Exp:0x0 Act:0x1
```

These External loopback diagnostics are interpreted as follows:

```
O/E Ext      --- module name: Plug-In Interface Module with
External Loop 155 Mb Loop Elec 155 Mb: type of diag run
LOS          --- type of failure: Loss of Signal(LOS)
Exp:0x0      --- expected value: 0 (no LOS present)
Act:0x1      --- actual value: 1 (LOS was present)
```

After running the System Internal diagnostics:

```
O/E Int 155 Mb Loop Elec 155 Mb
             LOS  Exp:0x0  Act:0x1

O/E Int 622 Mb Loop Opt 622 Mb
             LOS  Exp:0x0  Act:0x1
```

The Internal diagnostic results are interpreted the same as the External diagnostics with the module name changed to O/E Int.

After running the Protocol Board diagnostics:

```
Proto Bd 155 Mb Loop Elec 155 Mb
             LOS  Exp:0x0  Act:0x1

Proto Bd 622 Mb Loop Opt 622 Mb
             LOS  Exp:0x0  Act:0x1
```

The Protocol board diagnostic results are interpreted the same as the External diagnostics with the module name changed to Proto Bd.

Match these results against the Troubleshooting Sequence table. (Failures occurred in the Plug-In Interface Module Internal and External tests, and in the Protocol Board Loopback test.) The best match for these diagnostic results is at step 43.

Step 43 lists the following boards as possible suspects:

1. High Speed Protocol board
2. Main Protocol board (low probability)
3. Clock Generator board (low probability)

Since the High Speed Protocol board is listed as the highest probability for causing the problem, replace this board first. The High Speed and Main Protocol boards are considered a single unit and should be replaced as a single unit. After replacing the High Speed Protocol board, run all of the diagnostics again.

If there are no diagnostic failures after replacing a board, the Protocol boards were faulty. If the same diagnostic failures occur, the original Protocol boards should be reinstalled and the Clock Generator board should be replaced. After replacing the Clock Generator board, all the diagnostics should be run again.

If there are no diagnostic failures, the Clock Generator board was at fault. If the same diagnostic failures occur, the original Clock Generator board should be replaced in the instrument. Since all of the suggested sources of problems have been tested and the problem still remains, the instrument should be returned to the factory for service. A complete history of all attempts at problem resolution should be sent along with the instrument.

Troubleshooting Notes

Bus Faults can occur during any diagnostic. These faults are characterized by the following message:

```
BUS ERROR At Addr: 0xXXXXXX, (STTX Reg 3: 0xXX)
```

If a message like the above appears in any diagnostic failure display, it should be treated as a bus fault and not as a failure by the specific diagnostic.

If you have a large number of diagnostic failures, verify that the Low Voltage Power Supply is working.

You can run all of the diagnostics in loops to help isolate intermittent problems. Since some circuitry only produces failures under temperature stress, run the diagnostics at the same temperature that is causing the problems.

The entries in the Troubleshooting Sequence procedure are listed in order of probability of causing a problem.

After-Repair Adjustments

After the removal and replacement of a module, some adjustment may be required. Table 6–17 lists the adjustments required.

Table 6–17: Adjustments Required for Module Replaced

Module Replaced	Adjustment Required
Display Assembly	None required
Backplane Assembly	None required
CPU Assembly	Set the serial number, clock, and calendar
Auxiliary Power Supply	None required
Clock Generator Assembly	None required
Main Protocol Assembly	None required
High Speed Protocol Assembly	None required
Tributary Assembly	Calibrate Jitter (if option 14 is installed)
JAWA/JAWG Assemby	Calibrate Jitter
Optical or Electrical Interface Module	Calibrate Jitter (if option 14 is installed)
Low Voltage Power Supply	Adjust the display monitor
Monitor Assembly	Adjust the display monitor

Repackaging Instructions

If you ship the CTS, pack it in the original shipping carton and packing material. If the original packing material is not available, package the CTS as follows:

1. Obtain a corrugated cardboard shipping carton with inside dimensions at least 15 cm (6 in) taller, wider, and deeper than the CTS. The shipping carton must be constructed of cardboard with 170 kg (375 pound) test strength.
2. If you are shipping the CTS to a Tektronix field office for repair, attach a tag to the CTS showing its owner and address, the name of the person to contact about the CTS, the CTS type, and the serial number.
3. Wrap the CTS with polyethylene sheeting or equivalent material to protect the finish.
4. Cushion the CTS in the shipping carton by tightly packing dunnage or urethane foam on all sides between the carton and the CTS. Allow 7.5 cm (3 in) on all sides, top, and bottom.
5. Seal the shipping carton with shipping tape or an industrial stapler.

Options

Table 7–1 lists options you may find installed in the CTS 700-Series Test Sets.

Table 7–1: CTS 700-Series Test Set Options

Option	Description
Option 03	Optical/Electrical Plug-In Interface Module, 1310 nm, IR, 52 Mb and 155 Mb
Option 04	Optical/Electrical Plug-In Interface Module, 1310 nm, IR, 52 Mb, 155 Mb, and 622 Mb
Option 05	Optical/Electrical Plug-In Interface Module, 1550 nm, LR, 52 Mb, 155 Mb, and 622 Mb
Option 06	Optical/Electrical Plug-In Interface Module, 1310/1550 nm, 52 Mb, 155 Mb, and 622 Mb
Option 14	Jitter and Wander Generation and Analysis
Option 22 (CTS 710 only)	DS1/DS3 Add/Drop/Test Option
Option 36 (CTS 750 only)	2, 34, 140 Mb/s Add/Drop/Test Option

In addition, the following items can be ordered by their nine-digit Tektronix part numbers:

- Optical Connector Kit, part number 020–1885–XX
- Tributary Signal Converter/Attenuator, part number 067–0250–XX

For information about power cord options refer to Table 2–2, on page 2–2.

Electrical Parts List

The modules that make up this instrument are often a combination of mechanical and electrical subparts. Therefore, all replaceable modules are listed in the *Mechanical Parts List* section. Refer to that section for part numbers when using this manual.

Diagrams

This section contains an interconnect diagram and a block diagram for the CTS. Refer to *Theory of Operation* on page 3–1 for more information about the field-replaceable modules shown in the block diagram.

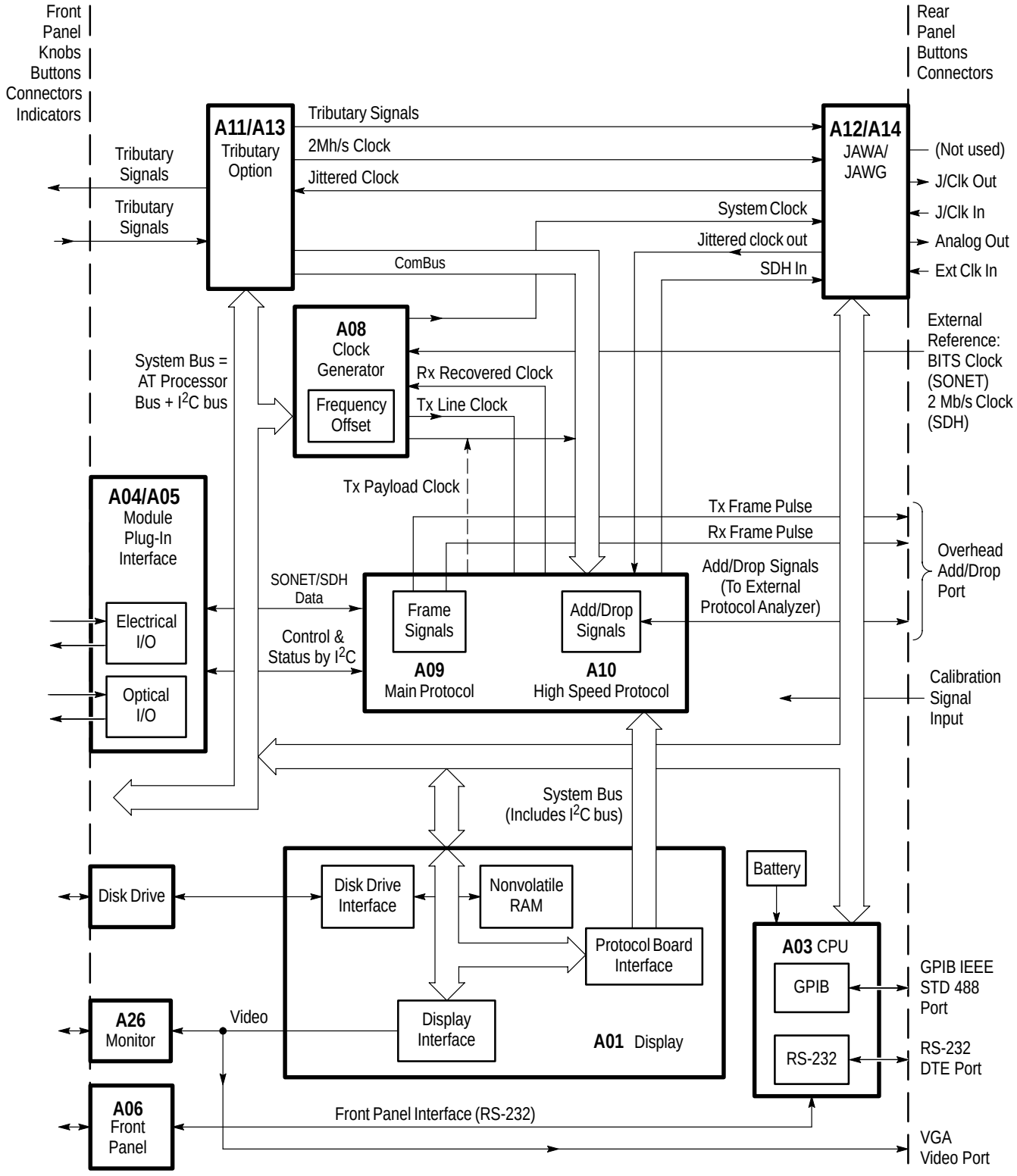
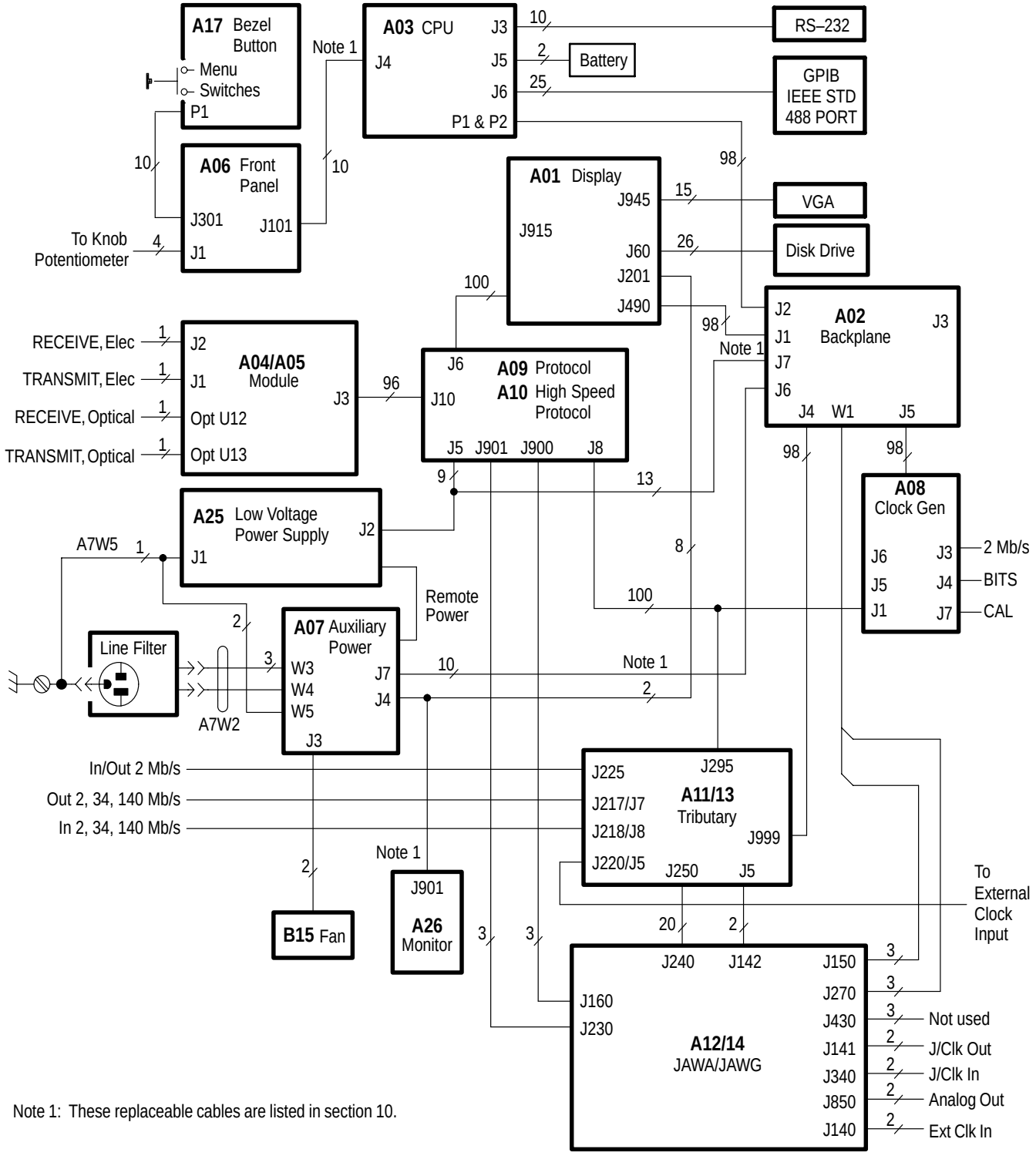


Figure 9–1: CTS Block Diagram



Note 1: These replaceable cables are listed in section 10.

Figure 9–2: CTS Interconnect Diagram

Mechanical Parts List

This section contains a list of the modules that are replaceable for the CTS. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. service center or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If a part you order has been replaced with a different or improved part, your local Tektronix service center or representative will contact you concerning any change in the part number.

Change information, if any, is located at the rear of this manual.

Module Replacement

The CTS is serviced by module replacement so there are three options you should consider:

- **Module Exchange.** In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1–800–TEKWIDE, ext. 6630.
- **Module Repair.** You may ship your module to us for repair, after which we will return it to you.
- **New Modules.** You may purchase new replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

The tabular information in the parts list is arranged for quick retrieval. Understanding the structure and features of the list will help you find all the information you need for ordering replacement parts.

Item Names

In the parts list, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, U.S. Federal Cataloging Handbook H6–1 can be used where possible.

Indentation System

This parts list is indented to show the relationship between items. The following example is of the indentation system used in the Description column:

1 2 3 4 5 Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
(END ATTACHING PARTS)
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
(END ATTACHING PARTS)
Parts of Detail Part
Attaching parts for Parts of Detail Part
(END ATTACHING PARTS)

Attaching parts always appear at the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. Attaching parts must be purchased separately, unless otherwise specified.

Abbreviations

Abbreviations conform to American National Standards Institute (ANSI) standard Y1.1.

CROSS INDEX – MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S3109	FELLER	72 VERONICA AVE UNIT 4	SUMMERSET NJ 08873
S3629	SCHURTER AG H C/O PANEL COMPONENTS CORP	2015 SECOND STREET	BERKLEY CA 94170
S4246	JAPAN SERVO CO LTD	7 KANDA MITOSHIRO–CHO CHIYODA–KU	TOKYO JAPAN
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609–3320
TK0860	LABEL GRAPHICS	6700 SW BRADBURY CT	PORTLAND OR 97224
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1547	MOORE ELECTRONICS INC	19500 SW 90TH CT PO BOX 1030	TUALATIN OR 97062
TK1694	ROSE CITY LABEL COMPANY	7235 SE LABEL LANE	PORTLAND OR 972069339
TK1857	HIROSE ELECTRIC USA INC	2688 WESTHILLS COURT	SIMI VALLEY CA 93065–6235
TK1891	PRESTOLE CORP	34589 GLENDALE ST	LIVONIA MI 48150–1303
TK1908	PLASTIC MOLDED PRODUCTS	4336 SO ADAMS	TACOMA WA 98409
TK1918	SHIN–ETSU POLYMER AMERICA INC	1181 NORTH 4TH ST	SAN JOSE CA 95112
TK1935	ACCRA–FAB INC	11007 NE 37TH CIRCLE	VANCOUVER WA 98682
TK1943	NEILSEN MANUFACTURING INC	3501 PORTLAND ROAD NE	SALEM OR 97303
TK2248	WESTERN MICRO TECHNOLOGY	1800 NW 169TH PL SUITE B–300	BEAVERTON OR 97006
TK2432	UNION ELECTRIC	15/F #1, FU–SHING N. ROAD	TAIPEI TAIWAN ROC
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE #2	VANCOUVER WA 98601
TK2539	ROYAL CASE COMPANY INC	315 S MONTGOMERY PO BOX 2231	SHERMAN TX 75070
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
TK2647	INSTRUMENT SPECIALTIES CO INC.	C/O TEMCO NW 1336 SE 51ST STREET	HILLSBORO OR 97123
TK6122	SELECTRON INC	7225 SW BONITA	TIGARD OR 97224
0D1M6	NMB TECHNOLOGIES INC	9730 INDEPENDENCE AVE	CHATSWORTH CA 91311
0DWW6	SPM/MICRO POWER ELECTRONICS	22990 NW BENNETT ST	HILLSBORO OR 97124
0DWW6	MICRO POWER ELECTRONICS	7973 SW CIRRUS DRIVE BLDG. #22	BEAVERTON OR 97005
0GV52	SCHAFFNER EMC INC	9–B FADEM ROAD	SPRINGFIELD NJ 07081
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661–2999
0KBZ5	Q & D PLASTICS INC	1812 – 16TH AVENUE PO BOX 487	FOREST GROVE OR 97116–0487
0KBZ5	MORELLIS Q & D PLASTICS	1812 16TH AVE	FOREST GROVE OR 97116
0KB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
0KB05	NORTH STAR NAMEPLATE	5750 NE MOORE COURT	HILLSBORO OR 97124–6474
00PZ4	EAC SHIELDING	13620 IMPERIAL HWY UNIT #7	SANTA FE SPRING CA 90670
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG PA 17105–3608
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039–2410

CROSS INDEX – MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
1DM20	PARLEX CORP	7 INDUSTRIAL WAY	SALEM NH 03079
14949	TROMPETER ELECTRONICS INC	31186 LA BAYA DR	WESTLAKE VILLAGE CA 91362–5069
18565	CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801–1039
2W733	COOPER INDUSTRIES INC BELDEN DIVISION	2200 US HIGHWAY 27 SOUTH PO BOX 1980	RICHMOND IN 47375–0010
22670	GM NAMEPLATE INCORPORATED	2040 15TH AVE WEST	SEATTLE WA 98119–2783
26003	MODULAR DEVICES INC	4115 SPENCER STREET	TORRANCE CA 90503–2489
30817	INSTRUMENT SPECIALTIES CO INC	EXIT 53 RT 80 BOX A	DELAWARE WATER GAP PA 18327
34416	PARSONS MFG CORP	1055 OBRIAN DR	MENLO PARK CA 94025–1408
50356	TEAC AMERICA INC	7733 TELEGRAPH RD PO BOX 750	MONTEBELLO CA 90640–6537
50463	POWER SYSTEMS INC.	45 GRIFIN ROAD	SOUTH LINFIELD CT 06002
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
56501	THOMAS & BETTS CORPORATION	1555 LINFIELD RD	MEMPHIS TN 38119
59730	THOMAS AND BETTS CORP	1555 LINFIELD RD	MEMPHIS TN 38141
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
61935	SCHURTER INC	1016 CLEGG COURT	PETALUMA CA 94952–1152
70674	ADC PRODUCTS DIV MAGNETC CONTROLS CO		
71400	BUSSMANN	DIVISION COOPER INDUSTRIES INC PO BOX 14460	ST LOUIS MO 63178
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–1							
–1	390–1133–00			1	CABINET,SCOPE:W/FOOT & SHIELDING	80009	390113300
–2	348–0764–04			1	SHLD GSKT,ELEK:0.125 X 0.188,WIRE MESH,2LAYERS,37L	18565	ORDER BY DESC
–3	200–3991–02			1	COVER,PANEL:HARD, POLYCARBONATE, LEXAN	80009	200399102
–4	334–8722–00			1	MARKER,IDENT:REAR COVER FUSE DATA W/ CE LABEL (ALL CTS 710)	80009	334872200
	334–8722–00		B040277	1	MARKER,IDENT:REAR COVER FUSE DATA W/ CE LABEL (ALL CTS 750)	80009	334872200
	334–9444–00	B040278	B059999	1	MARKER,IDENT:REAR COVER FUSE DATA, W/ CE LABEL (CTS 750 W/O OPTION 14)	0KB05	334–9444–00
	334–9528–00	B040278	B059999	1	MARKER,IDENT:REAR COVER FUSE DATA, W/O CE LABEL (CTS 750 OPTION 14)	0KB05	334–9528–00
	334–9444–00	B060000		1	MARKER,IDENT:REAR COVER FUSE DATA, W/ CE LABEL (ALL CTS 750)	0KB05	334–9444–00
–5	343–1213–00			1	CLAMP,PWR CORD:POLYMIDE (STANDARD ACCESSORY)	TK1163	ORDER BY DESC
–6	159–0014–00			1	FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC, (AMERICAN)	61857	SS2–5A
	159–0255–00			1	FUSE,CARTRIDGE:FAST BLOW,4A,125V (EUROPEAN)	61857	EQ4A
	159–0046–00	B040278		1	FUSE,CARTRIDGE:3AG,8A,250V,15SEC,CER (ALL CTS750)	71400	ABC 8
–7	200–2264–00			1	CAP,FUSEHOLDER:3AG FUSES (AMERICAN)	61935	FEK 031 1666
	200–2265–00			1	CAP,FUSEHOLDER:5 X 20MM FUSES (EUROPEAN)	61935	FEK 031.1663
–8	334–8676–00			1	MARKER,IDENT:JITTER/WANDER (OPTION 14)	0KB05	334–8676–00
–9	334–8672–00			1	MARKER,IDENT:OPTIONS	0KB05	334–8672–00
–10	334–8668–00			1	MARKER,IDENT:REARCOVER OVERHEAD ADD/DROP	80009	334866800
–11	334–5258–00			1	MARKER,IDENT:MKD X–RAY WARNING,GERMAN,	TK1694	ORDER BY DESC
–12	211–0691–00			4	SCREW,MACHINE:6–32 X 0.625,PNH,STL	0KB01	ORDER BY DESC
–13	348–1219–00			2	FOOT,REAR:SANTOPRENE	80009	348121900
–14	161–0230–01			1	CABLE ASSY,PWR,:3,18 AWG,92 L,SVT,TAN (STANDARD ACCESSORY)	TK2432	ORDER BY DESC
–15	367–0356–01			1	HANDLE,CARRYING:POLYCARBONATE LEXAN 500R	80009	367035601
–16	212–0144–00			2	SCREW,TPG,TF:8–16 X 0.562,PLASTITE,SPCL HD	0KB01	ORDER BY DESC
–17	348–0659–00			2	FOOT,CABINET:BLACK POLYURETHANE	0JR05	ORDER BY DESC
–18	211–0730–00			1	SCR,ASSEM WSHR:6–32X0.375 PNH STL CD PL	0KB01	ORDER BY DESC

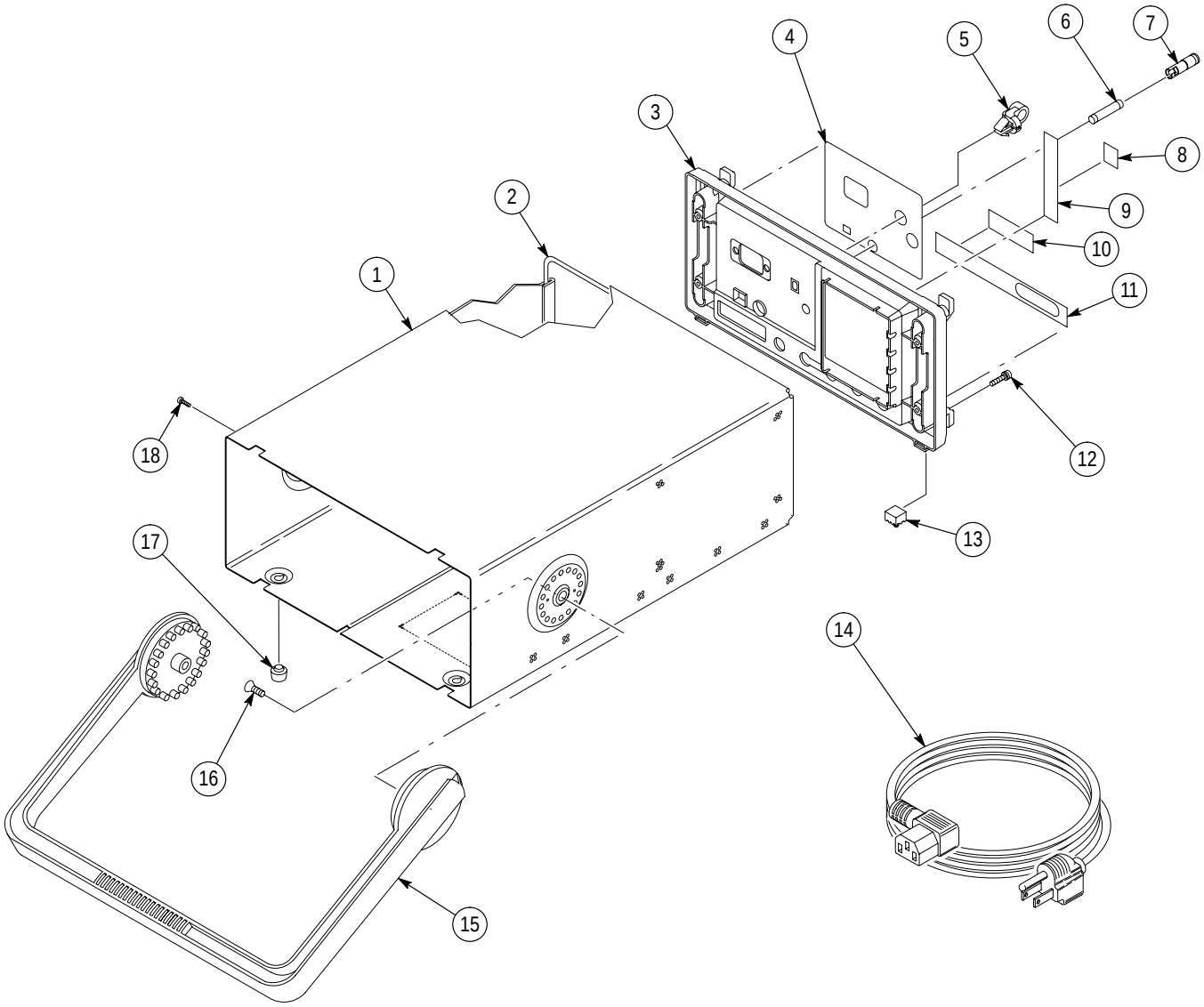


Figure 10–1: Cabinet and Rear Panel

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–2							
–1	334–8633–00			1	MARKER,IDENT:BEZEL,CTS710	80009	334863300
	334–8640–00			1	MARKER,IDENT:BEZEL,CTS750	80009	334864000
–2	354–0734–01			1	TRIM,RING:FRONT,WITH ACRYLIC CRT FILTER	80009	354073401
–3	366–2176–00			12	PUSH BUTTON:MENU BUTTON	TK1163	ORDER BY DESC
	366–0752–00			1	PUSH BUTTON:MENU BUTTON W/ TEXT	TK1163	ORDER BY DESC
–4	260–2539–00			1	SWITCH,SET:,ELASTOMERIC BEZEL	TK1918	260–2539–00
–5	259–0086–00			1	FLEX CIRCUIT:BEZEL BUTTON	07416	ORDER BY DESC
–6	348–1408–00			1	GASKET,SHIELD:EMI,CLIP–ON,8.5L	80009	348140800
–7	348–1258–00			4	SHLD,GASKET,ELE:2 LAYER,0.094 X 0.188 X 8.750 (CTS710)	80009	348125800
	348–1409–00			3	GASKET,SHIELD:ELECTRONIC,0.094 X 0.250 X8.75 (CTS750)	00PZ4	348140900
–8	672–1364–51			1	CIRCUIT BD ASSY:FRONT PANEL MODULE (STD)	80009	672136451
	672–0360–50			1	CIRCUIT BD ASSY:FRONT PANEL MODULE (OPTION 22)	80009	672036050
	672–0361–50			1	CIRCUIT BD ASSY:FRONT PANEL MODULE (OPTION 36)	80009	672036150
–9	366–2175–00			1	KEYCAP:PUSH BUTTON,1.25 H X 0.3 X0.4	80009	366217500
–10	174–3439–00			2	CA ASY,SP:COAXIAL,75 OHM,6.375 L,BNC	53387	174–3439–00
–11	105–1081–00	B030375		1	BRACKET,ADAPTER:FLOPPY DISK DRIVE (CTS710 Only)	80009	105108100
		B030225			(CTS750 Only)		
–12	211–0840–00			1	SCREW,MACHINE:M2.6 X 0.45MM X 4.0MM L,PHIL,PNH	0KB01	26C4MXPHY
–13	672–1404–04	B010100	B020280	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (STANDARD)	80009	672140404
	672–1445–02			1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (STANDARD)	80009	672144502
	672–1404–04	B010100	B020165	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (STANDARD)	80009	672140404
	672–1445–02			1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (STANDARD)	80009	672144502
	672–1403–08	B010100	B020280	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (OPTION 03 ONLY)	80009	672140308
	672–1444–00	B020281		1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (OPTION 03 ONLY)	80009	672144400
	672–1403–08	B010100	B020165	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (OPTION 03 ONLY)	80009	672140308
	672–1444–00	B020166		1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (OPTION 03 ONLY)	80009	672144400
	672–1420–04	B010100	B020280	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (OPTION 04 ONLY)	80009	672142004
	672–1441–00	B020281		1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS710 (OPTION 04 ONLY)	80009	672144100
	672–1420–04	B010100	B020165	1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (OPTION 04 ONLY)	80009	672142004
	672–1441–00	B020166		1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (OPTION 04 ONLY)	80009	672144100
	672–1439–03			1	CIRCUIT BD ASSY:ELECTRICAL MODULE CTS750 (OPTION 05 ONLY)	80009	672143903
–14	200–3091–00			2	COVER,DUST:W/BEAD CHAIN,FC STYLE	TK1857	HRFC–C1
–15	200–3232–02			1	COVER,FRONT:ASB	TK1908	ORDER BY DESC

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
–16	119–4547–00	B010100	B030374	1	DISK DRIVE:FLOPPY,3.5 INCH;2MB,0.5 INH DSDD (CTS710 Only)	TK2248	119–4547–00
		B010100	B030224		(CTS750 Only)		
	119–5413–00	B030375			DISK DRIVE:FLOPPY,3.5 INCH;2MB,0.5 INH DSDD (CTS710 Only)	80009	119–5413–00
		B030225			(CTS750 Only		
–17	366–2099–01			1	KNOB:TAN,BLANK,0.25 X 1.375 X 0.4	TK1163	ORDER BY DESC

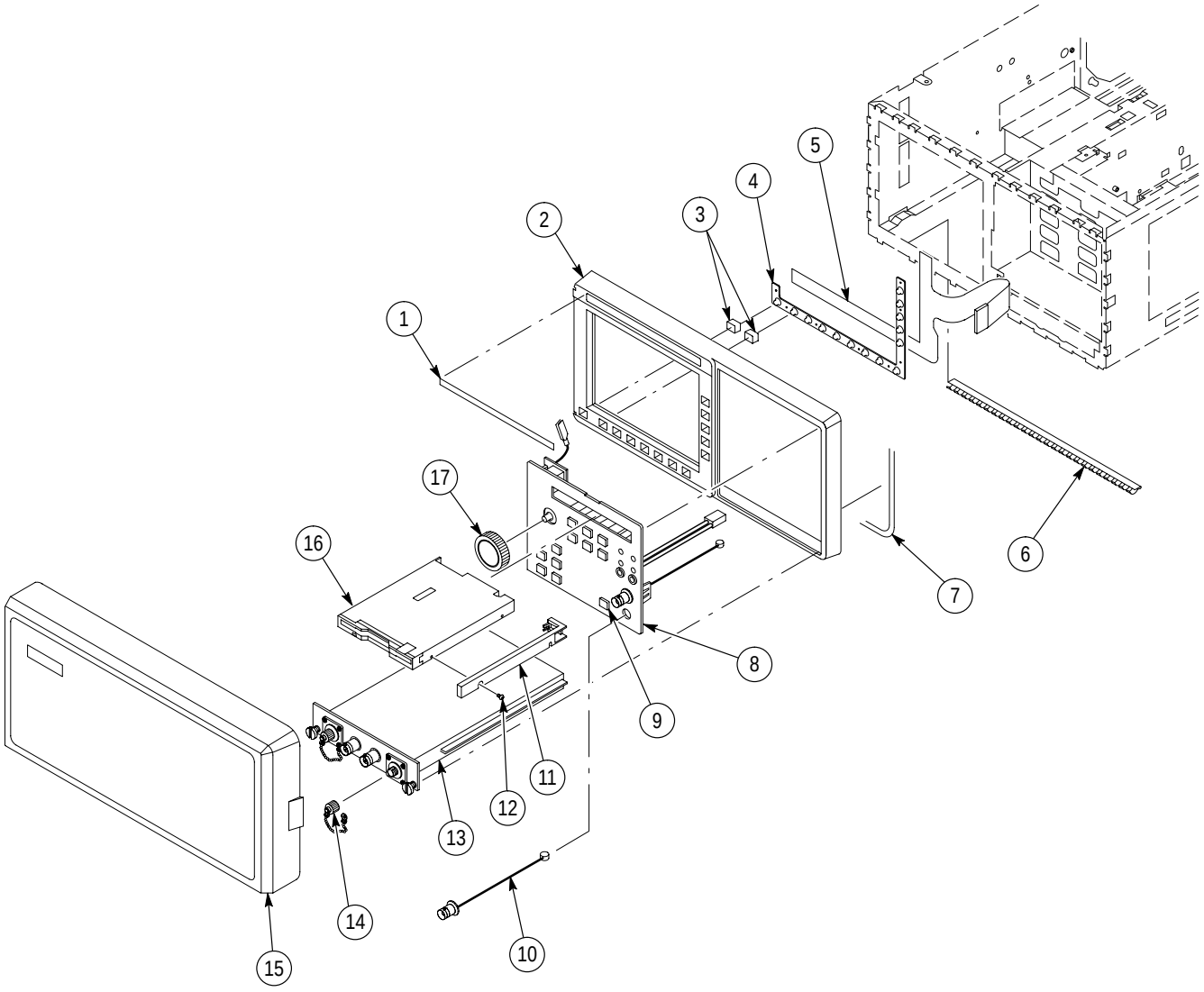


Figure 10–2: Front Panel

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–3							
–1	407–4442–00			1	BAFFLE,AIR:AIR BAFFLE,ALUM,3.600 INCHES	TK1935	407–4442–00
–2	211–0718–00			1	SCREW,MACHINE:6–32 X 0.312,FLH100,CDPL	0KB01	ORDER BY DESC
–3	211–0722–00			3	SCREW,MACHINE:6–32 X 0.250,PNH,STL,CDPL,T–15	0KB01	ORDER BY DESC
–4	213–0882–00			22	SCREW,TPG,TR:6–32 X 0.437,PNH,STL,CDPL,TYPETT	0KB01	ORDER BY DESC
–5	426–2426–00			1	FRAME,FAN MTG:POLYCARBONATE	TK1163	426–2426–00
–6	200–2264–00			1	CAP,FUSEHOLDER:3AG FUSES	S3629	FEK031 1666
–7	204–0906–00			1	BODY,FUSEHOLDER:3AG & 5X20MM FUSES	S3629	TYPE FAU 031.35
–8	679–4086–00			1	CIRCUIT BD ASSY:AUXILARY POWER	80009	679408600
	671–4139–00	B040278		1	CIRCUIT BD ASSY:AUXILARY P0WER, (CTS 750 ONLY)	TK6122	671–4139–00
–9	119–1770–04			1	FAN,DC:TUBEAXIAL;12V,2.0W,49.5 CFM,40 DBA,7.5" LEAD	S4246	CUDC12D4 MK3*
	119–5602–00	B030375		1	FAN,DC:TUBEAXIAL, 12V, 6.84W, 90 CFM, 39 DBA, (CTS710 ONLY)	0D1M6	DC 4710NL–04W–B50–D00
	119–5602–00	B040278		1	FAN,DC:TUBEAXIAL, 12V, 6.84W, 90 CFM, 39 DBA, (CTS750 ONLY)	0D1M6	DC 4710NL–04W–B50–D00
–10	119–5549–00			1	POWER SUPPLY:175W,90–250VAC	26003	119–5549–00
	119–5557–00	B040278		1	POWER SUPPLY:225W, 90–132/180–250VAC, (CTS750 ONLY)	26003	119–5557–00
–11	386–6159–00			1	SUPPORT,CKT BD:BACK PLANE & PWR SPLY,PC	TK1163	386–6159–00
–12	119–5028–00			1	FILTER,RFI:4A,250V,48 TO 440HZ	80009	119502800
	119–5636–00	B040278		1	FILTER,RFI:10A,115–240V,DC – 400HZ, (CTS 750 ONLY)	0GV52	FN9223–10–06
–13	407–4032–00			1	BRACKET.CKT BD:BLANK	80009	407403200
	407–4301–00			1	BRACKET,DSP:DSP & FILLER, W/PEM NUTS	80009	407430100
–14	386–6158–00			1	SUPPORT,CKT BD:MAT MATERIAL	80009	386615800
–15	146–0056–02			1	BATTERY:3V,1200MAH,2/3A LITHIUM BATTERY ASSY,6.250	0DWW6	ORDER BY DESC
–16	211–0840–00	B010100	B030374	2	SCREW,MACHINE:M2.6 X 0.45MM X 4.0MM L,PHIL,PNH (CTS710 Only)	0KB01	26C4MXPHY
		B010100	B030224		(CTS750 Only)		
		B030375		1	(CTS710 Only)		
		B030225			(CTS750 Only)		
	211–0866–00	B030375		1	SCREW PHIL M2.5X10 PHIL PNH BRZN (CTS710 Only)	0KB01	211–0866–00
		B030225			(CTS750 Only)		
–17	344–0116–00			1	RTNR,CAPACITOR:0.625 DIA,STEEL	TK1891	E50003–007
–18	671–2755–51			1	CIRCUIT BD ASSY:PROTOCOL	80009	671275551
	671–3607–51	B030375		1	CIRCUIT BD ASSY:PROTOCOL (CTS710 ONLY)	80009	671360751
	671–3607–51	B030225		1	CIRCUIT BD ASSY:PROTOCOL (CTS750 ONLY)	80009	671360751
–19	129–0851–00			4	SPACER,POST:0.709 L,6–32 INT/EXT,SST,0.25 HEX0.475 L	0KB01	129–0851–00
–20	671–2826–52			1	CIRCUIT BD ASSY:HIGH SPEED PROTOCOL	80009	671282652
	671–3572–51	B030375		1	CIRCUIT BD ASSY:HIGH SPEED PROTOCOL, (CTS 710 ONLY)	80009	671357251
	671–3572–51	B030225		1	CIRCUIT BD ASSY:HIGH SPEED PROTOCOL, (CTS 750 ONLY)	80009	671357251
–21	348–1412–00			1	GASKET,EMI:W/ADNESIVE	30817	348–1412–00

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
–22	348–1552–00			1	GASKET,EMI:LONGITUDINAL GND STRIP,COPPER,3.906 INCHES L,CLIP ON	TK2647	0097097617 CUT TO 3.906 L
–23	131–1247–00			1	TERM,QIK DISC.:0.187 X 0.02 BLADE,45 DEG BEND	00779	61664–1
–24	441–2044–01			1	CHASSIS ASSY:ALUMINUM	TK1935	441–2044–01
	441–2044–02	B060000		1	CHASSIS ASSY:ALUMINUM (CTS750 ONLY)	TK1935	441–2044–02
–25	211–0732–00	B010100	B030375	1	SCR,ASSEM WSHR:6–32 X 0.75,PNH,STL,CD PL,TORX T15 (CTS710 ONLY)	0KB01	ORDER BY DESC
		B010100	B030225		(CTS750 ONLY)		
–26	426–2436–01			1	FRAME,CRT FLTR:POLYCARBONATE	TK1163	ORDER BY DESC
–27	348–1291–00			2	SHLD,GSK ELEK:CLIP–ON EM GASKET	30817	9760–5090–20
–28	640–0079–03			1	DISPLAY MONITOR:7 INCH,480X640 PIXEL	80009	640007903

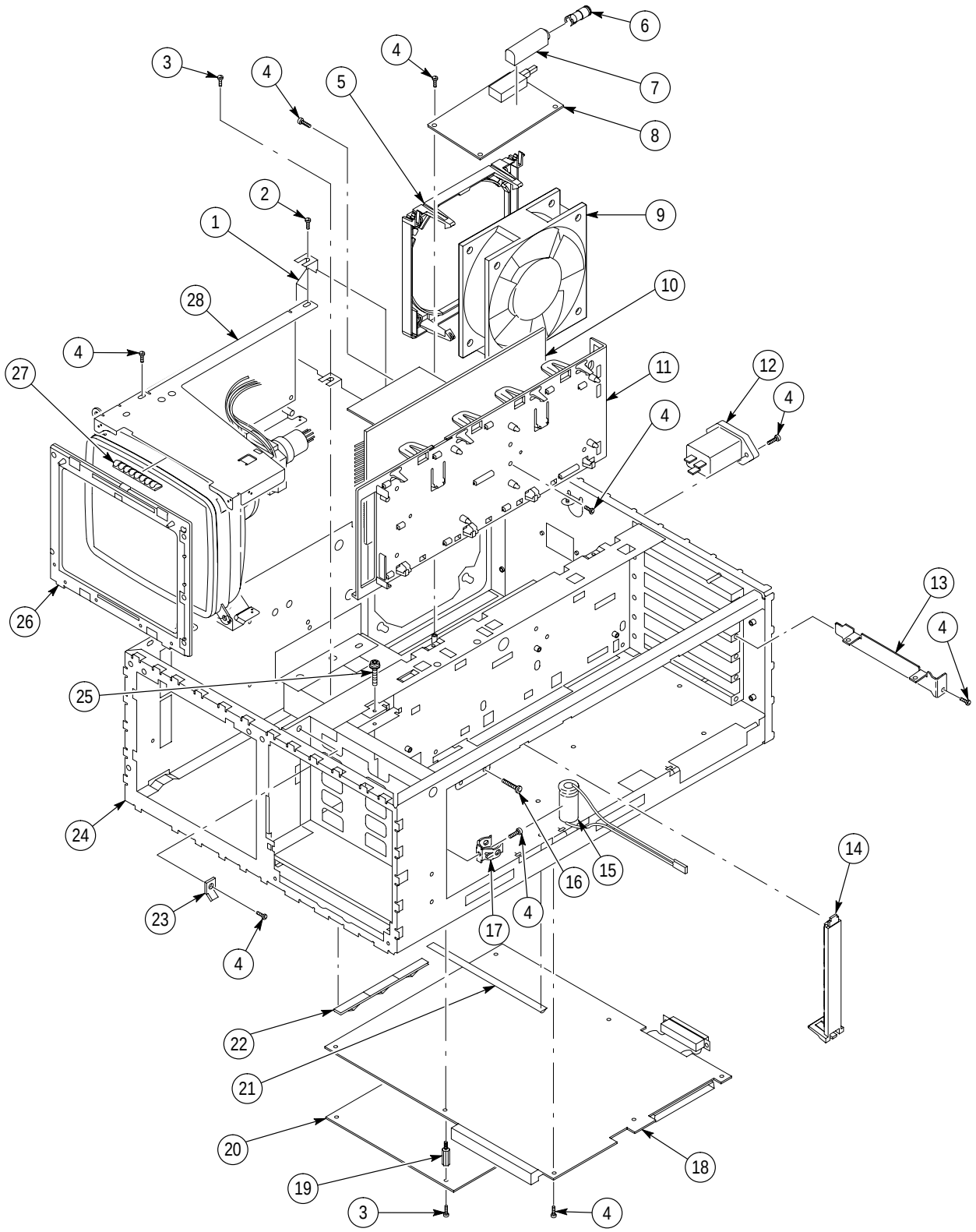


Figure 10–3: CRT and Mainframe

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–4							
–1	200–3660–00			1	COVER,AUTO CAL:POLYCARBONATE	TK1163	ORDER BY DESC
–2	334–3003–00			1	MARKER,IDENT:MKD DANGER	TK0860	ORDER BY DESC
–3	337–4138–00			1	SHIELD,EMI:ALUM	80009	337413800
–4	213–0882–00			22	SCREW,TPG,TR:6–32 X 0.437,PNH,STL,CDPL,TYPETT	0KB01	ORDER BY DESC
–5	213–1079–00			2	JACKSCREW:4–40 X 0.250EXT THD		
–6	671–2541–50			1	CIRCUIT BD ASSY:DISPLAY	80009	671254150
–7	671–2653–06			1	CIRCUIT BD ASSY:CPU (CTS710 ONLY	80009	671265306
	671–2653–26			1	CIRCUIT BD ASSY:CPU (CTS750 ONLY)	80009	671265326
–8	672–1457–51			1	CIRCUIT BD ASSY:JAWA/JAWG (CTS750 OPTION 14 ONLY)	80009	672145751
–9	671–3260–50			1	CIRCUIT BD ASSY:DS1/DS2 ADD/DROP TEST TRIBUTARY (CTS710 OPTION 22 ONLY)	80009	671326050
	671–3259–51			1	CIRCUIT BD ASSY:E1/E3 ADD/DROP TEST TRIBUTARY (CTS750 OPTION 36 ONLY)	80009	671325951
–10	174–3308–00			1	CA ASSY,SP:RIBBON,IDC,14,28 AWG,1.75 L	TK2469	174–3308–00
–11	174–3599–00			1	CA ASSY, RF:COAX,RFD,75 OHM, MMS TO MMS,3.8 L	53387	ORDER BY DESC
–12	174–3563–00			1	CA ASSY, RF:COAX,RFD,75 OHM,MMS TO MMS,2.8L	TK2469	174–3563–00
–13	174–3178–00			2	CA ASSY,SP:SHLD CMPST,TLC,2,TW PR,100 OHM DIFF	53387	174–3178–00
–14	174–3733–00			1	CA ASSY,SP:DISCRETE,CPD,22AWG,10.0L	TK2469	174–3733–00
–15	671–3601–51			1	CIRCUIT BD ASSY:CLOCK GENERATOR	80009	671360151
–16	671–2991–03			1	CIRCUIT BD ASSY:BACKPLANE	80009	671299103
–17	346–0133–00			1	STRAP,TIEDOWN,E:14.0 X 0.091,NYLON	59730	TY234M EURO DIR
–18	348–0150–00			1	GROMMET,PLASTIC:DK GRAY,U–SHAPE,0.66 ID	0KBZ5	348015000

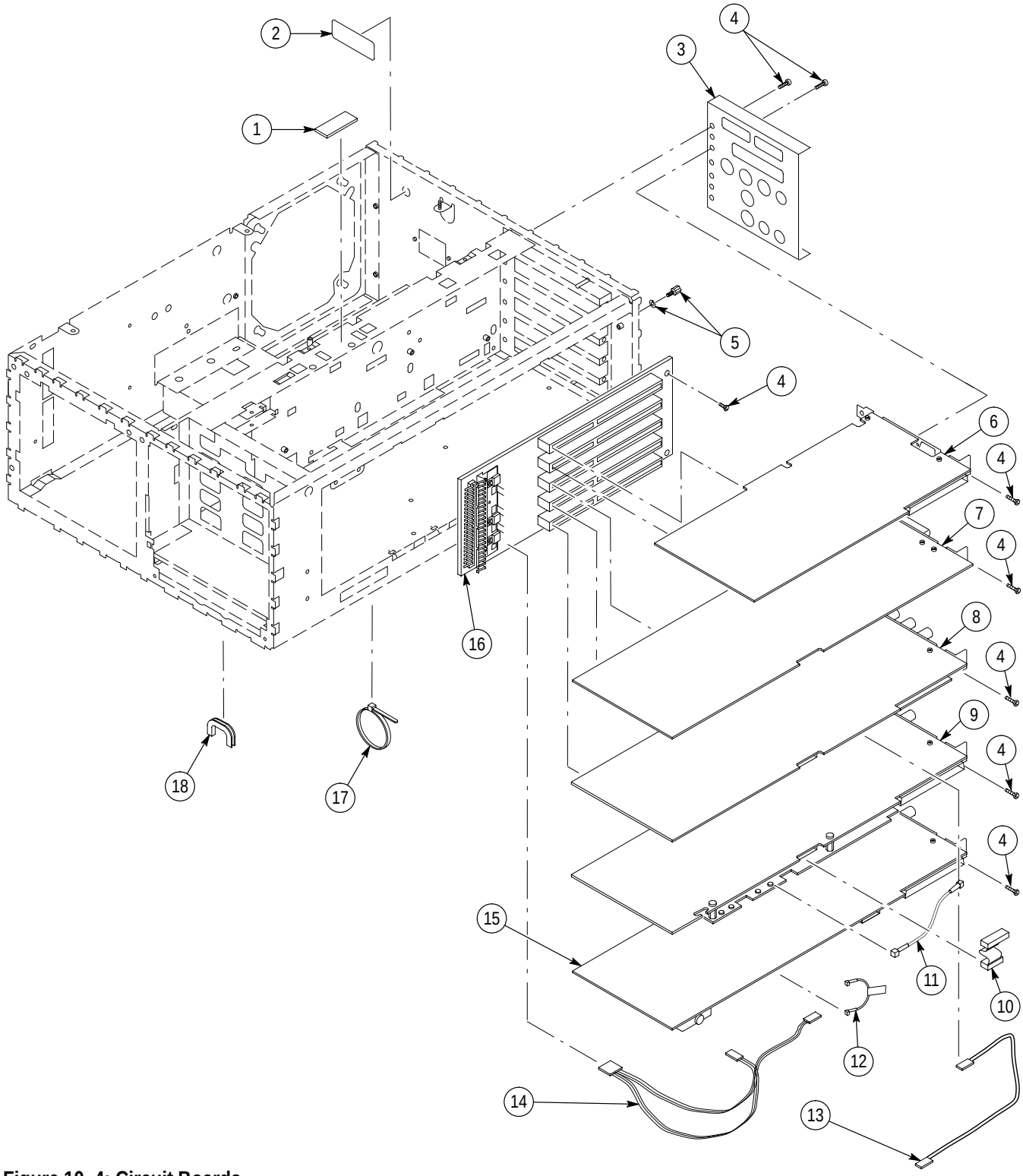


Figure 10–4: Circuit Boards

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–5					**CTS 710 CABLES**		
–1	174–3044–00			1	CA ASSY,PWR:DESCRETE,;PSC,22,18 AWG,1X22	TK2469	174–3044–00
–2	174–2282–00			1	CA ASSY,SP:FLAT FLEX,;FLX,10,26 AWG,15.8 L	TK2469	174–2282–00
–3	174–2283–00			1	CA ASSY,SP:FLAT FLEX,FLX,10,26AWG,11.0L	TK2469	174–2283–00
–4	174–2288–00			1	CA ASSY,PWR:DESCRETE,;PSC,18 AWG,3.5 L,RTANG,0.25	TK2469	174–2288–00
–5	210–0457–00			2	NUT,PL,ASSEM WA:6–32X0.312,STL CD PL	TK0435	ORDER BY DESC
–6	174–2631–00			1	CA ASSY PWR:DESCRETE,;PSC,3,18 AWG,1X5,0.156 CTR	TK2469	174–2631–00
–7	174–3040–02			1	CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR	53387	ORDER BY DESC
–8	174–3039–00			1	CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR,9.0 L	53387	ORDER BY DESC
–9	174–3038–00			1	CA ASSY,SP:RIBBON,;IDC/MLD,10,28 AWG,0.05 CTR,1.75 L	53387	174–3038–00
–10	174–2964–01			1	CA ASSY SP:FLAT FLEX,26,COND,300 V,1.5A,8.0 L	1DM20	174–2964–01
10–6					**CTS 750 CABLES**		
–1	174–3044–01			1	CA ASSY,PWR:DESCRETE,;PSC,22,18 AWG,1X22	TK2469	174–3044–00
–2	174–2282–00			1	CA ASSY,SP:FLAT FLEX,;FLX,10,26 AWG,15.8 L	TK2469	174–2282–00
–3	174–2288–00			1	CA ASSY,PWR:DESCRETE,;PSC,18 AWG,3.5 L,RTANG,0.25	TK2469	174–2288–00
–4	210–0457–00			2	NUT,PL,ASSEM WA:6–32X0.312,STL CD PL	TK0435	ORDER BY DESC
–5	174–2631–00			1	CA ASSY PWR:DESCRETE,;PSC,3,18 AWG,1X5,0.156 CTR	TK2469	174–2631–00
–6	174–3040–02			1	CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR	53387	ORDER BY DESC
–7	174–3039–00			1	CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR,9.0 L	53387	ORDER BY DESC
–8	174–3038–00			1	CA ASSY,SP:RIBBON,;IDC/MLD,10,28 AWG,0.05 CTR,1.75 L	53387	174–3038–00
–9	174–3699–00			1	CA ASSY,SP:FLAT FLEX,FLEX,27 AWG,6.0 L	TK2469	174–3699–00
–10	174–2283–00			1	CA ASSY,SP:FLAT FLEX,FLX,10,26AWG,11.0L	TK2469	174–2283–00
–11	174–2964–01			1	CA ASSY SP:FLAT FLEX,26,COND,300 V,1.5A,8.0 L	1DM20	174–2964–01

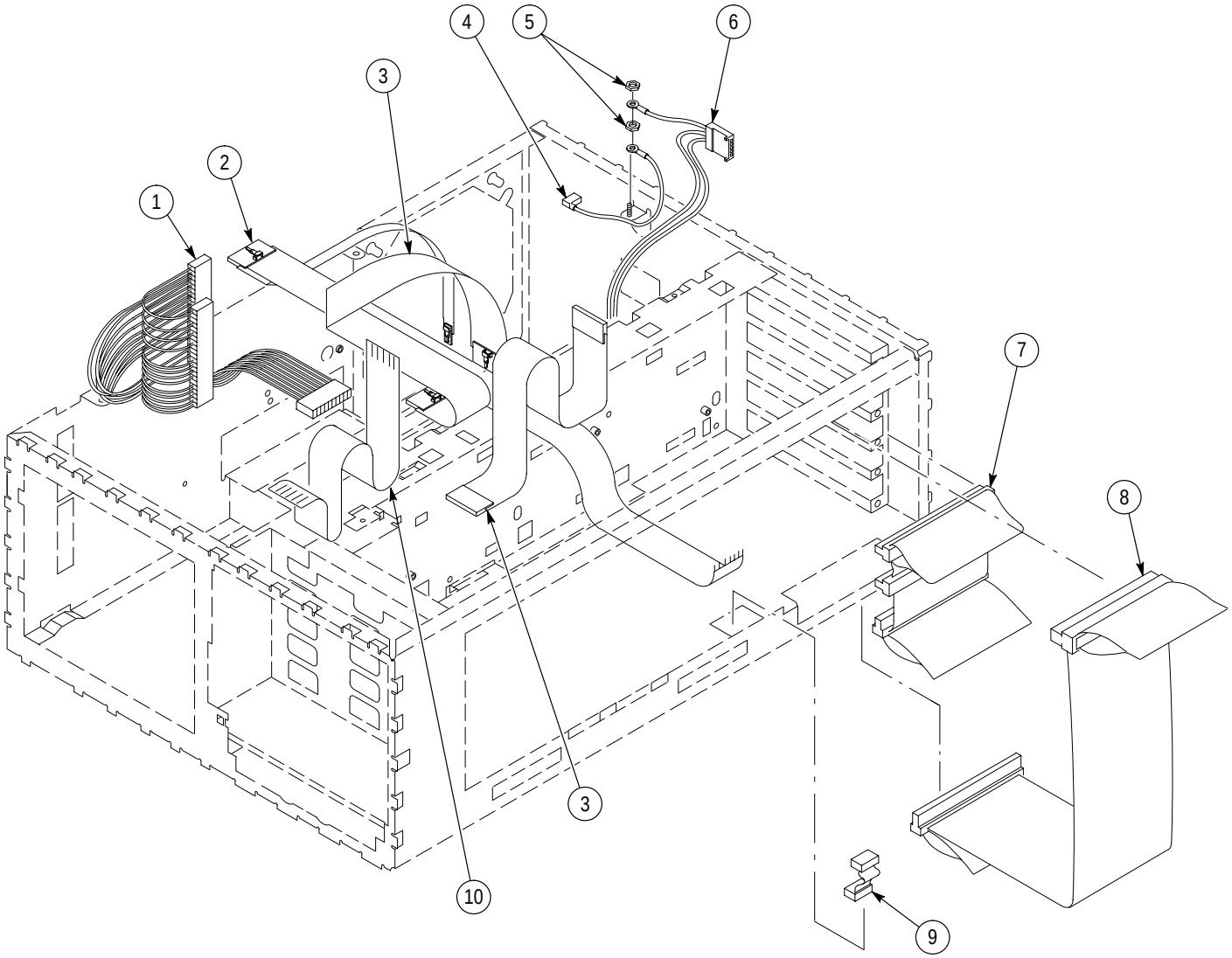


Figure 10–5: CTS 710 Cables

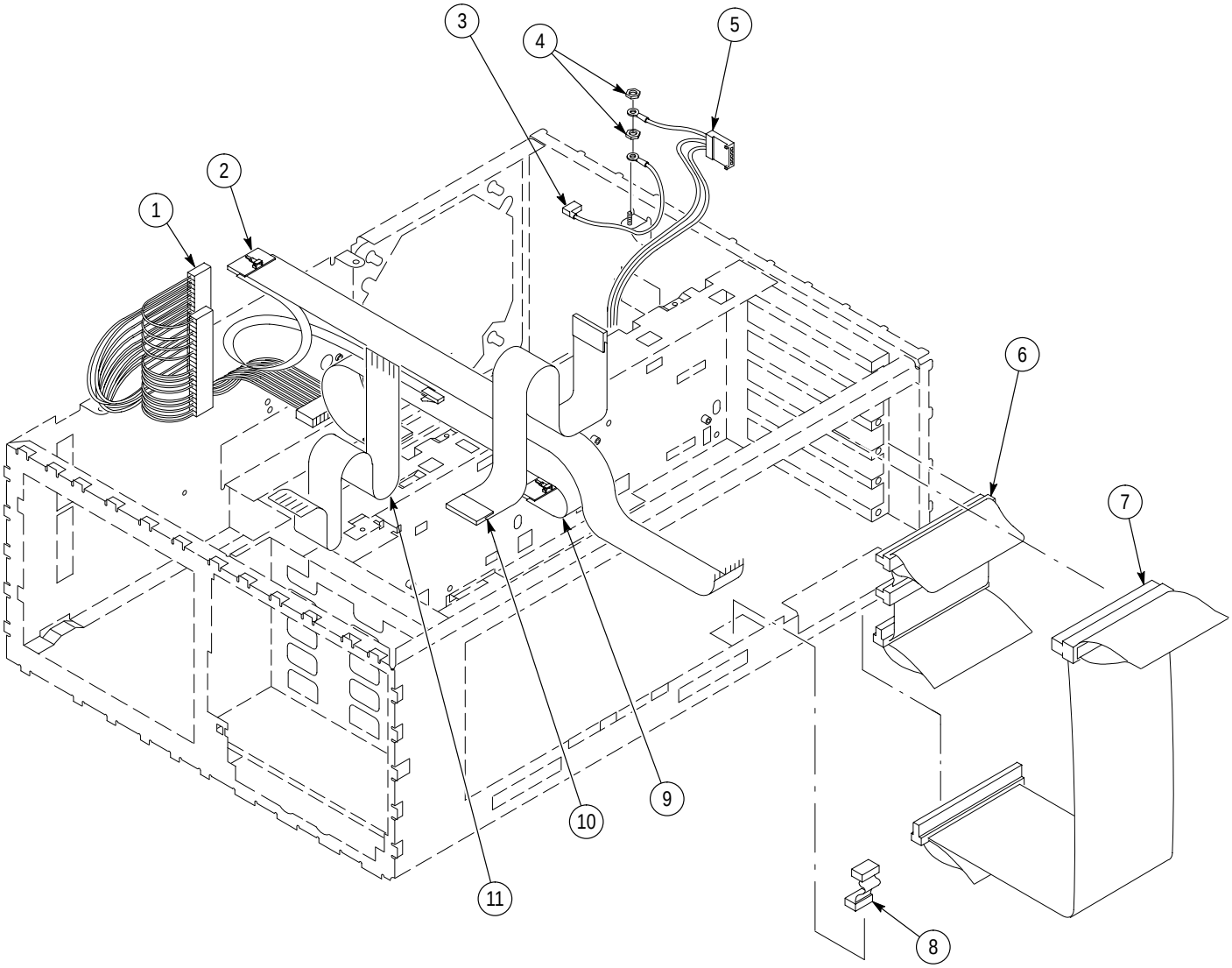


Figure 10–6: CTS 750 Cables

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10–7					**STANDARD ACCESSORIES**		
–1	161–0230–XX			1	CABLE ASSY,PWR,:3,18 AWG,92 L,SVT,TAN,60 DEG (STANDARD–SEE FIGURE 10–1–12)		
–2	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG (OPTION A3–AUSTRALIAN)	S3109	ORDER BY DESC
–3	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG (OPTION A1–EUROPEAN)	S3109	ORDER BY DESC
–4	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG (OPTION A2–UNITED KINGDOM)	S3109	ORDER BY DESC
–5	161–0104–08			1	CA ASSY,PWR:3,18 AWG,250/10A,98 INCH L,RTANG (OPTION A4–NORTH AMERICAN)	2W733	ORDER BY DESC
–6	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG (OPTION A5–SWITZERLAND)	S3109	ORDER BY DESC
–7	343–1213–XX			1	CLAMP,PWR CORD:POLYMIDE (SEE FIGURE 10–1–5)		
	343–0170–00			1	RTNR,CA TO CA:U/W 0.25 OD CABLES (OPTIONS A1,A2,A3,A4,A5)	0JR05	ORDER BY DESC
	200–2265–00			1	CAP,FUSEHOLDER:5 X 20MM FUSES (OPTIONS A1,A2,A3,A4,A5)	61935	FEK 031.1663
	070–8852–XX			1	MANUAL,REF:USER,CTS710	TK2548	070–8852–XX
	070–8921–XX			1	MANUAL,REF:USER,CTS750	TK2548	070–8921–XX
	070–8854–XX			1	MANUAL,REF:PROGRAMMER:REFERENCE	TK2548	070–8854–XX
	070–8924–XX			1	MANUAL,TECH:PROGRAMMER,CTS710	TK2548	070–8924–XX
	070–8925–XX			1	MANUAL,TECH:PROGRAMMER,CTS750	TK2548	070–8925–XX
	070–9336–XX			1	MANUAL,TECH:REFERENCE,ENGLISH,CTS710	TK2548	070–9336–XX
	070–9337–XX			1	MANUAL,TECH:REFERENCE,ENGLISH,CTS750	TK2548	070–9337–XX
					OPTIONAL ACCESSORIES		
	012–1469–00			1	CABLE,SIEMENS:CMPST,DIN41628;SDI,3,120 OHM,BAL	TK2469	012–1469–00
	012–1470–00			1	CABLE,INTCON:COAX,PATCH CORD;SDI,75 OHM,6.0L	70674	CC1756
	012–1471–00			1	CABLE,INTCON:COAX,;SDI,75 OHM,6.0 L,BNC,MALE	70674	CC1656
	016–1157–00			1	CASE,CARRYING:26 X 22 X 12,HARD TRANS W/WHEELS	34416	ORDER BY DESC
	016–1158–00			1	CASE,CARRYING:SOFT PADDED,OPTIONS	80009	016115800
	070–8853–XX			1	MANUAL,TECH:SERVICE	TK2548	070–8852–XX
	070–9338–XX			1	MANUAL,TECH:REFERENCE,FRENCH,CTS750	TK2548	070–9338–XX
	070–9339–XX			1	MANUAL,TECH:REFERENCE,GERMAN,CTS750	TK2548	070–9339–XX
	070–9713–XX			1	MANUAL,TECH:REFERENCE,ITALIAN,CTS750	TK2548	070–9713–XX
	070–9770–XX			1	MANUAL,TECH:REFERENCE,SPANISH,CTS750	TK2548	070–9770–XX
	103–0365–00			1	ADAPTER,CONN RF:DSI BANTAM–WECO310 ADAPTER	70674	AP051
	103–0366–00			1	ADAPTER,CONN:BNC–WECO 440,;BNC	14949	ADMW12
	103–0367–00			1	ADAPTER,CONN:BNC–WECO 358;BNC,JACK,75 OHM	14949	AD1W

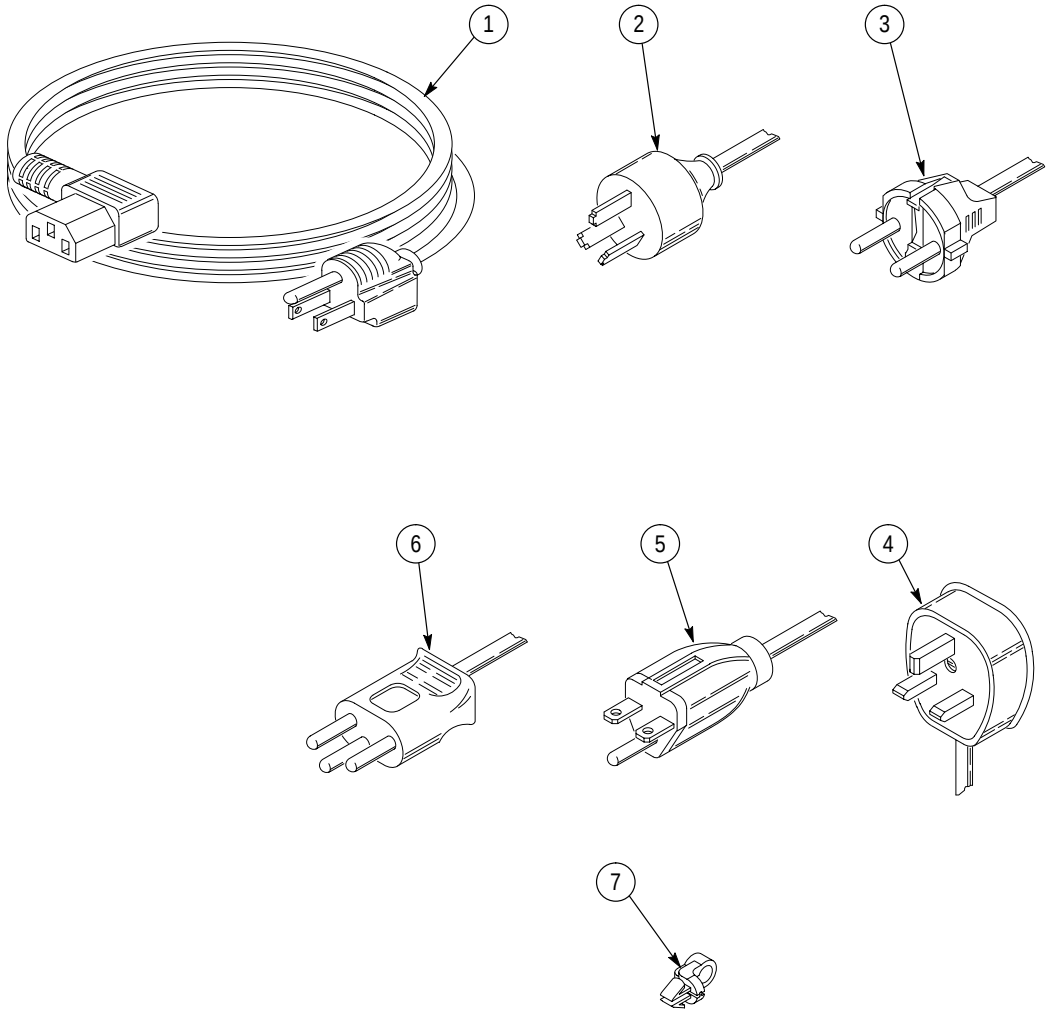


Figure 10–7: Power Cords

Glossary

AIS
An acronym for Alarm Indication Signal. An AIS is used to alert downstream equipment that an upstream failure has been detected.

APS
An acronym for Automatic Protection Switching.

ASCII
An acronym for American Standard Code for Information Interchange.

BER
An acronym for Bit Error Ratio (or Rate). The principal measure of quality of a digital transmission system. BER is defined as

$$BER = \frac{Number\ of\ Errors}{Total\ Number\ of\ Bits}$$

BER is usually expressed as a negative exponent. For example, a BER of 10^{-7} means that 1 bit out of 10^{7} bits is in error.

BIP
An acronym for Bit Interleaved Parity. A method used to monitor errors in the transmitted signal.

Bit Error
An incorrect bit. Also known as a coding violation.

BITS
An acronym for Building Integrated Timing Supply.

Coding Violation (CV)
A coding violation is an error detected by Bit-Interleaved Parity (BIP) checks.

COFA
An acronym for Change of Frame Alignment.

dB
The symbol for Decibels.

dBm
The symbol for power level in decibels relative to 1 mW.

DM
An acronym for Degraded Minute. A degraded minute is a minute with a BER greater than 1 E-6.

DSn
An acronym for Digital Signal-n (DS1, DS2, and DS3). DS1 is the basic multiplex rate in North America.

Digital Signal Transmission Rates

Level	Rate	Multiple of DS1
DS1	1.544 Mbps	1
DS1c	3.152 Mbps	2
DS2	6.312 Mbps	4
DS3	44.736 Mbps	24

E1, E2, E3, E4
Alternative names for the CCITT 2 Mb/s, 8 Mb/s, 32 Mb/s, and 140 Mb/s tributary signals.

EFS
An acronym for Error Free Seconds.

Errored Seconds – Type A
The number of seconds that contained only one CV and no defects.

Errored Seconds – Type B
The number of seconds that contained more than one and less than X CVs and no defects. The range for X depends on the transmit rate, but corresponds to a BER of $\approx 10^{-6}$.

ES
An acronym for Errored Second. A second with at least one error.

FEBE
An acronym for Far End Block Error. An indication returned to the transmitting LTE that an errored block has been detected at the receiving LTE.

FERF
An acronym for Far End Receive Failure. A FERF indicates to the transmitting LTE that the receiving LTE has detected an incoming line failure or is receiving a Line AIS.

HO Path
An abbreviation for High Order Path.

Line
The portion of a transmission line between two multiplexers.

Line Alarm Indication Signal (AIS)
A Line AIS is generated by Section Terminating Equipment upon loss of input signal or loss of frame.

Line Far End Receive Failure (FERF)
An indication returned to a transmitting LTE from the receiving LTE that a Line AIS or incoming line failure has been detected.

Line Coding Violations (CVs)
Line CVs are the sum of the BIP errors detected at the Line layer. Line CVs are collected using the BIP codes in the B2 bytes of the Line overhead.

Line Errored Seconds (ESs)
A Line ES is a second during which at least one Line CV, or a second during which the line was in the Line AIS state.

Line Severely Errored Seconds (SESs)
A Line SES is a second with N or more Line CVs, or a second during which the line was in the Line AIS state. The value of N varies with the transmit rate, but corresponds to a BER of $\approx 10^{-6}$.

LOF
An acronym for Loss of Frame.

LOP
An acronym for Loss of Pointer.

LOS
An acronym for Loss of Signal.

LTE
An acronym for Line Terminating Equipment.

Mb/s
An abbreviation for megabits per second.

mapping
The process of placing a tributary signal into a SONET SPE or an SDH AU.

NE
An acronym for Network Element.

OC
An acronym for Optical Carrier.

Optical Carrier Level N (OC-N)
An optical version of an STS-N signal.

OOF
An acronym for Out of Frame.

Path
The portion of a SONET/SDH transmission network between two terminal multiplexers.

Path Overhead (POH)
A set of bytes allocated within the information payload (SPEVC) to carry status and maintenance information between terminal equipment along the same path as the information.

POH
An acronym for Path Overhead.

PTE
An acronym for Path Terminating Equipment.

Rx
An abbreviation for Receive.

SDH
An acronym for Synchronous Digital Hierarchy.

Section
The portion of a transmission line between a Network Element (NE) and a Line Terminating Equipment (LTE) or two LTEs.

Section Coding Violations (CVs)
Section CVs are BIP errors that are detected at the Section layer. CVs for the Section layer are collected using the BIP-8 in the B1 byte located in the Section overhead of STS-1 number 1.

Section Errored Seconds (ESs)
A Section ES is a second during which at least one Section CV or OOF/COFA event occurred, or a second during which the NE was (at any point during the second) in the LOS state.

Section Overhead
A set of bytes allocated within each frame to carry framing and error monitoring information between repeaters along the same path as the information.

Severely Errored Seconds (SESs)
An SES is a second with more than X CVs, where X corresponds to a BER of $\approx 10^{-6}$; or a second with one or more defects in the layer.

SES
An acronym for Severely Errored Seconds.

SOH
An acronym for Section Overhead.

SONET
An acronym for Synchronous Optical NETwork.

SPE
An acronym for Synchronous Payload Envelope.

STE
An acronym for Section Terminating Equipment.

STM-N
An acronym for Synchronous Transport Module–N (STM-1, -4, -16). The different STM-N rates are listed in the following table. The table below also includes the ANSI (American National Standards Institute) designation for the equivalent SONET (Synchronous Optical NETwork) rates.

SDH/SONET Signal Hierarchy

		SONET Designation	
SDH Designation	Data Rate (Mb/s)	Electrical Signal	Optical Signal
	51.84	STS-1	OC-1
STM-1	155.52	STS-3	OC-3
STM-4	622.08	STS-12	OC-12
STM-16	2488.32	STS-48	OC-48

STS
An acronym for Synchronous Transport Signal.

STS-N
An acronym for Synchronous Transport Signal level-N (STS-1, -3, -12, -24, -48). The different STS-N rates (and their optical equivalents) are listed in the following table. The table below also includes the CCITT Synchronous Digital Hierarchy (SDH) designation for the equivalent SONET rates. The SDH standard refers to signals as Synchronous Transport Modules-N (STM-N).

SONET/SDH Signal Hierarchy

SONET Designation		Data Rate (Mb/s)	SDH Designation
Electrical Signal	Optical Signal		
STS-1	OC-1	51.84	
STS-3	OC-3	155.52	STM-1
STS-12	OC-12	622.08	STM-4
STS-48	OC-48	2488.32	STM-16

Tributary
The lower rate signal input to a multiplexer for combination (multiplexing) with other low rate signals to form a higher rate signal.

TU
An acronym for Tributary Unit (SDH).

TUG
An acronym for Tributary Unit Group (SDH).

TE
An acronym for Terminal Equipment.

Through Mode
The ability to retransmit the incoming signal without changing its contents.

TOH
An acronym for Transport Overhead. 1.728 Mb of bandwidth allocated within the information payload to carry status and maintenance information end to end between terminal equipment along the same path as the information.

Transport Overhead
A set of bytes allocated within each frame to carry status and maintenance information between terminal equipment along the same path as the information.

Tx
An abbreviation for Transmit.